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(54) **Display and its driving method**

Anzeigevorrichtung und Verfahren zu ihrer Steuerung

Dispositif d'affichage et méthode de commande

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a display and its driving method, and more particularly to a display and its driving method for inputting the image signal of various standards into the panel having only a predefined number of rows.

Related Background Art

[0002] Nowadays, provision of information in society has rapidly progressed such that multi-media are in much demand. Particularly, a thin type flat display as the computer to human interface, in place of CRT (Cathode Ray Tube), becomes an important device to extend the multi-media market. As the flat display, an LCD (Liquid Crystal Display), a PDP (Plasma Display) and an electron beam flat display are widely accepted. Particularly, the liquid crystal display has gained large market along with the spread of small-sized personal computers. Among the liquid crystal displays, an active matrix liquid crystal display has greater contrast over the whole screen because of having no crosstalk, as compared with a simple matrix liquid crystal display such as STN. Therefore, the active matrix liquid crystal display has drawn public's attention not only as the display for small personal computers, but also as the view finder for video camera, the projector, and the thin type television.

[0003] The active matrix liquid crystal display is classified into TFT and diode types. Fig. 32A is a block diagram of the image signal input for TFT image display. 220 is a display pixel unit having pixels arranged in a matrix, 240 is a vertical scan circuit for selecting the display row, 230 is a sampling circuit for color image signal, and 280 is a horizontal scan circuit for outputting the sampling signal.

[0004] A unit pixel of the display pixel unit 220 is composed of a switching element 211, a liquid crystal material 215 and a pixel capacitor 212. When the switching element 211 is a TFT (thin film transistor), a gate line 213 connects the gate electrode of TFT to the vertical scan circuit 240, one terminal of pixel capacitor 212 for each of all the pixels being connected commonly to a common electrode 221 of an opposed substrate, to which a common electrode voltage V_{LC} is applied. When the switching element 211 is a diode (including Metal/Insulator/Metal element), the scan electrode runs transversely across the opposed substrate to connect to the vertical scan circuit 240 An input terminal of the switching element 211 is connected by a vertical data line to the sampling circuit 230. Whether TFT or diode, a vertical data line 214 connects the input terminal of the switching element 211 to the sampling circuit 230 and an output terminal of the switching element 211 connected to the other terminal of the pixel capacitor 212.

[0005] A control circuit 2140 separates an image signal into necessary signals for the vertical scan circuit 240 the horizontal scan circuit 280 or a signal processing circuit 2120. The signal processing circuit 120 performs a gamma processing in view of the liquid crystal characteristics, or an inversion signal processing for the longer life of liquid crystal to output a color image signal (red, blue, green) to the sampling circuit 230.

[0006] Fig. 32B is a detail equivalent circuit diagram of the display pixel unit 220 and the sampling circuit 230 for TFT color. 210 is a unit pixel for each color. The pixels (R, G, B) are arranged in delta configuration, the same color being allocated on either side of the data line 214 (d1, d2,...) for every row, and connected to the data line 214(d1, d2,...). The sampling circuit 230 is comprised of switching transistors (sw1, sw2,...) and capacitors (parasitic capacitor and pixel capacitor of the data line 214). An image signal input line 216 is comprised of a signal line dedicated for each color of RGB. The switching transistors (sw1, sw2,...) sample each color signal from the image signal input line 216 in accordance with a pulse (ϕh1, ϕh2,...) from the horizontal scan circuit280, and transfer each color signal to each pixel through the data line 214 (d1, d2,...). And they send pulses (ϕg1, ϕg2,...) from the vertical scan circuit 40 to the TFT gate of pixels, and write a signal into each pixel by selecting the row. In this way, the pulse (ϕg1, ϕg2,...) turns on the TFT 211 contained in each row, so that the image signal for one horizontal scan in each corresponding row is written into all pixels contained in each row. It is noted that the image signal for one horizontal scan is thereafter referred to as 1H signal.

[0007] The liquid crystal display displays a television signal or a personal computer signal, but there are a variety of standards for these signals, whereby it is necessary to normally fabricate the panel for liquid . crystal display of the type conforming to respective standard. On the other hand, there is a liquid crystal display for displaying the signal of various standards on one panel through an appropriate signal processing. For example, a liquid crystal display is provided which displays the image of PAL (Phase Alternation by Line) system having more scan lines than the NTSC (National Television System Committee) system on the panel only having the rows corresponding to the number of scan lines in the NTSC system. Such display examples were disclosed in Japanese Laid-Open Patent Application No. 2-182087 or Japanese Laid-Open Patent Application No. 5-37909. In these publications, a processing of thinning out some 1H signals from the image signal according to the PAL system is adopted. Specifically, in order to transform the effective number of scan lines 280 for one field in the PAL system into 240 lines of the NTSC system, the image signal is thinned out at a rate of 1 line for every 7 lines. Fig. 33 represents a specific example of this thinning out method. The image signal of PAL system is written on a liquid crystal display only having the

rows for one field (i.e., half rows of one frame) of the NTSC system. If the image signal of NTSC system is input, 1H signal o1, o2,... for odd field, or 1H signal e1, e2,... for even field is written sequentially into each row (L1, L2,...) for the liquid crystal display. If the image signal of PAL system is input, the thinning out processing is performed, because there are more scan lines than the NTSC system. As an enable circuit erases a write instruction into the row (L9) upon a horizontal gate pulse which the vertical scan circuit outputs, 1H signal o7 (e9) is thinned out. And as 1H signal o8 (e10) is written for the next 1H period, 1H signal o7 (e9) is not displayed. Δ indicates a 1H signal which is thinned out. Beside, there are two-row simultaneous driving in which 1H signal is written into adjacent two rows on a panel having the rows of two field (i.e., one frame), and accordingly two-row interpolation driving. In this case, like the signal input onto the panel only having the rows for one field, the image signal of the standard of having more scan lines than one frame of the panel is displayed by completely thinning out particular 1H signals.

[0008] In the display as described above, there is a drawback that because 1H signal is completely thinned out, the image is distorted so that the character or fine line of image in the vertical direction on the screen is not displayed, particularly that the contour is less visible. To overcome this drawback of image distortion, there is disclosed a system in Japanese Laid-Open Patent Application No. 5-236453. This system once writes the image signal of interlace system into the memory for the conversion into the image signal of non-interlace system. And image distortion is moderated by thinning out only one row, instead of thinning out two rows conventionally. Also, the similar method was disclosed in Japanese Laid-Open Patent Application No. 5-100641.

[0009] On the other hand, when the image signal is input into the liquid crystal display, it is common that the image signal is made the alternating current to prevent the burning of liquid crystal material. Also, if the spatial distribution and the temporal distribution of the panel is observed microscopically, the central voltage is preferably 0. Namely, it is preferable that adjacent rows are reversely polarized, and the polarity in the same row is reversed in a short time. This is true with a plasma display and an electron beam flat display in which if deflected signal voltage is input for long time, the electrode is corroded and the element is deteriorated. In this respect, because Japanese Laid-Open Patent Application No. 5-236435 as above cited does not consider the image signal that is made the alternating current, the image signal of the same polarity succeeds in the row direction by making the scanning for thinning out, resulting in a possibility that if taking notice of three rows, the central voltage of the image signal will greatly deviate from 0. Also, the above-mentioned No. 5-100641 discloses a method of inputting the image signal having a different polarity for each row, but this method requires a large amount of memory, resulting in a complicated circuit. Thus, the present invention has a subject to provide a display capable of displaying the image signal of various standards while reducing image distortion associated with the scan for thinning out as much as possible, thereby inputting reversely the image signal optimally, only with the addition of a simple circuit.

SUMMARY OF THE INVENTION

[0010] The present inventors have achieved the following invention, as a result of assiduous efforts to accomplish the above subject.

[0011] According to a first aspect of the present invention, there is provided a method of driving a colour display panel as defined in the appended claim 1.

[0012] According to a second aspect of the present invention, there is provided a colour display apparatus as defined in the appended claim 6.

[0013] Fig. 1 shows an interlace circuit which is a portion of the driving means according to the present invention. 1 is a first control line, 2 is a second control line, 3 is a third control line, 1-1, 1-2, 1-3 is a first group of switches, 2-1, 2-2, 2-3 is a second group of switches, and 3-1, 3-2, 3-3 is a third group of switches. m1, m3, m5 is a line leading to a vertical scan circuit. By sending an appropriate pulse to the first control line connecting to the first group of switches, the second control line connecting to the second group of switches, and the third control line connecting to the third group of switches, the selection of row can be changed. Also, it is desirable to use a MOS transistor as the switch. The vertical scan circuit should be a bootstrap scan circuit. If the image signal constituting one frame by m horizontal scans is of the NTSC system, m is from 480 to 525. If the image signal constituting one field by k (k<m) horizontal scans to input the image is of the PAL system, k is from 250 to 313. Image signal input means normally writes the image signal corresponding to one horizontal scan, among k horizontal scans as above cited, into two rows, and only at every arbitrary n-th (n≤k) horizontal scan, writes the image signal corresponding to said n-th horizontal scan into any one row among said m rows. This value of n is desirably from 2 to 8, and more desirably from 3 to 4. The present invention is not limited to the NTSC system or PAL system, but also deal with the image signal of various standards. For example, VGA (Video Graphic Array; the number of rows 480), SVGA (Super Video Graphic Array; the number of rows 600), XGA (Xtended Graphics Array; the number of rows 768) and EWS (Engineering Work Station; the number of rows 1024) are acceptable.

[0014] The present invention can deal with any display as far as it is of the type sequentially scanning a multiplicity of rows by a scan circuit. Examples of the display of such type include a liquid crystal display, a plasma display, an electron beam flat display, an electroluminescence display and a multiluminous diode display. Among them, the present invention has a signifi-

cant advantage over the small-sized portable display because of the capability of displaying the image signal of various standards. Among these liquid crystal display, plasma display, and electron beam display, it is a liquid crystal display that is most portable, and it is most beneficial to apply the present invention to the liquid crystal display. This liquid crystal display is either of the active matrix type and the simple matrix type. However, it is an active matrix type liquid crystal display that allows the interpolation driving of multiple rows, for one data line, while connecting a plurality of pixels that are offset in the horizontal direction due to delta arrangement. For example, an example 1 as hereinafter described is illustrative thereof. A two-row simultaneous driving may be applied to both the simple matrix and the active matrix. The active matrix type liquid crystal display may be of two terminal type (MIM type), or three terminal type (TFT type).

[0015] Normally, 1H signal is displayed in multiple rows (the number of simultaneously selected rows is assumed p), but some 1H signal is displayed only in q (<p) rows when displayed. Especially, 1H signal is written into two rows, but certain 1H signal is written in only one row. Hence, even if the signal having necessary more rows as with the PAL system is input into a display only having less rows as with the NTSC system, there is no 1H signal to completely thin out. In this way, a display manufactured in the NTSC system can be made a display in the PAL system, and a display manufactured for the PAL can be made a display for the NTSC system. Therefore, it is possible to display the image signal of various standards on a single display. Also, the inversion input of image signal optimal for the panel can be effected only by the addition of a simple circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Fig. 1 shows an example of driving means of the present invention.

[0017] Fig. 2 is a block diagram showing the flow of image signal in an example 1.

[0018] Fig. 3 is a detail view of an interlace circuit and a line memory.

[0019] Fig. 4 is a chart showing the phase and polarity of image signal for each row on a panel.

[0020] Figs. 5A and 5B are examples of the timing chart.

[0021] Fig. 6 represents (a) sampling pulse in delta arrangement, (b) sampling pulse in aligned arrangement, and (c) inversion image signal.

[0022] Figs. 7A and 7B represent circuit diagram and voltage waveform for a bootstrap scan circuit.

[0023] Fig. 8 represents the voltage waveform generating the scan pulse.

[0024] Fig. 9 is a chart showing the phase and polarity of image signal for each row on a panel in an example 2.

[0025] Fig. 10 is a chart showing the phase and polarity of image signal for each row on a panel in an example 3.

[0026] Fig. 11 is a diagram showing a pixel array in an example 4.

[0027] Fig. 12 shows exemplary timing charts.

[0028] Figs. 13A and 13B represent a block diagram showing the flow of image signal in examples 5, 6, 7 and a detail diagram of a display unit.

[0029] Fig. 14 is a diagram showing the input of image signal.

[0030] Fig. 15 is a view showing the color array of pixel.

[0031] Fig. 16 shows exemplary timing charts.

[0032] Fig. 17 is a chart showing the image signal for each row on a panel in an example 5.

[0033] Fig. 18 is a diagram showing the input of image signal.

[0034] Fig. 19 is a view showing the color array of pixel.

[0035] Fig. 20 is a block diagram of an analog line memory.

[0036] Fig. 21 shows exemplary timing charts.

[0037] Fig. 22 is a chart showing the image signal for each row on a panel in an example 6.

[0038] Fig. 23 shows exemplary timing charts.

[0039] Fig. 24 shows exemplary timing charts.

[0040] Fig. 25 shows an example of a circuit for phasing image signal.

[0041] Fig. 26 shows exemplary timing charts.

[0042] Fig. 27 is a chart showing the input of image signal.

[0043] Fig. 28 is a block diagram of an analog line memory.

[0044] Fig. 29 shows exemplary timing charts.

[0045] Figs. 30A and 30B are typical views of an original signal image and an image in an example 7.

[0046] Fig.31 is a view showing an electron beam flat display.

[0047] Figs. 32A and 32B are block diagrams of the conventional flow of image signal and a detail diagram of pixel.

[0048] Fig. 33 is a chart showing the polarity of image signal for each row on a conventional panel.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0049] An example 1 is one in which the present invention is applied to the two-row interpolation driving which is effective for the pixels in delta arrangement. The two-row interpolation driving has two image input circuits. Fig. 2 is a block diagram showing the flow of image signal in this example. In the figure, 20 is a display pixel unit, 40 is a vertical scan circuit of the display pixel unit, 60 is an interlace circuit for row selection, 80-1, 80-2 are horizontal scan circuits for display pixel unit, 100-1, 100-2 are line memories for temporarily storing the image signal sampled, 120-1, 120-2 are signal processing circuits for gamma processing of image sig-

nal of inversion signal processing for electrical polarity to drive the liquid crystal, and 140 is a control circuit for driving the display device. S_1 and S_2 represent image signals which have undergone signal processing in different signal processing circuits 120-1, 120-2, respectively. Herein, the first image input circuit contains 80-1, 100-1, 120-1, and the second image input circuit contains 80-2, 100-2, 120-2.

[0050] Fig. 3 is a detail circuit diagram of the interlace circuit 60, the display pixel unit 20, and the line memories 100-1, 100-2. In the figure, 10 is a unit pixel consisting of a switching element, a liquid crystal and a color filter, D_1 to D_n are vertical signal lines (data lines), V_1 to V_n are signal lines from the vertical scan circuit, and L_1 to L_n are horizontal gate lines for the row selection. Also, 17 is a reset transistor, 18 is a temporary storage capacitor, and 19 is a switching transistor.

[0051] For example, if the V1 pulse gets H, a transistor connecting thereto conducts, so that the row selection can be arbitrarily made from three rows in terms of interlace pulses (or vertical selection pulses) ϕG, ϕGo, ϕGe. Accordingly, the interlace circuit allows for various drivings including the interlace, two-line simultaneous field row shift, and non-interlace.

[0052] Fig. 4 is a chart showing the image signal to be written into the pixel in the example 1. The panel row is indicated by L1, L2, ..., and the image signal to be written into corresponding row is indicated by o1, o2, ... in the odd field and e1, e2, ... in the even field for every 1H. At this time, the sampling phase of the signal to be written in each row pixel is indicated by A and B, and the inversion signal polarity is indicated by - and +. This sampling phase indicates a difference in the sampling timing.

[0053] Fig. 6 represents the sampling pulse from the shift register (80-1, 80-2) in (a) delta arrangement and (b) aligned arrangement.

[0054] As shown in Fig. 3, in a delta arrangement in which each color of R, G and B is shifted by 1.5 pixels between adjacent rows, to improve the horizontal resolution, it is necessary to change the sampling pulse phase by 180° for every row (a) in Fig. 6 Also, by changing the inversion signal polarity for every row, it is possible to reduce the flicker. Thus, if the sampling phase and the polarity of inversion signal for each image signal in a line memory 1 and a line memory 2 are made as shown in Fig. 4 the above object can be accomplished.

[0055] The writing of image signal in this example will be described in Fig. 4. An image signal A is sampled at the timing indicated by H_{1n}(A), and an image signal B is sampled at the timing indicated by H_{2n}(B) in (a) in Fig. 6. When writing image signal o1, o2, each 1H signal is alternately written by changing the sampling phase (e. g., a signal o1 at 1H is written on a row L_1 as o1A-, and on a row L_2 as o1B+). And during image compression to write an image signal o3, only one of 1H signal is written (a signal o3 at 3H is written on a row pixel L_5 as o3A-), but the other is not written (o3B+). The not written image signal is indicated by Δ. As a result, the image in the vertical direction is compressed. In this way, because o3 signal is not thinned out, the vertical resolution is not degraded. The next 4H signal is written as o4B+ on a row L_6 and o4A- on a row L_7 by the interlace circuit. Such normal driving and compression driving operation is performed for every several Hs in both the odd field and the even field.

[0056] Figs. 5A and 5B represent the timing charts in this example. Fig. 5B is an enlarged chart of a portion surrounded by the dot line in Fig. 5A. (c) in Fig.6 represents signal waveform examples of inversion image of a pixel. In the odd field, A phase, negative polarity signal is temporarily stored in the line memory 1, and B phase, positive polarity signal is temporarily stored in the line memory 2, these signals being then transferred to each row. In the figure, ϕH is a horizontal blanking pulse, ϕc is a residual charge reset pulse for selected pixel and vertical signal line, ϕGo, ϕGe, ϕG are interlace pulses, and V1, V2,.. are vertical scan pulses. The horizontal blanking pulse represents the synchronizing signal for the image signal. $\phi T1$ is a transfer pulse from the line memory (100-1) to selected row, and $\phi T2$ is a transfer pulse from the line memory 2 (100-2) to selected row. The interlace pulses V1, V2 represent selected rows at 1H and 2H.

[0057] If the vertical pulse V1 gets "H" at 1H, the image signal o1 is sampled in the line memory 1 and the line memory 2 during its effective scan period. The sampling timing is different in sampling phase between odd row and even row of row pixel, as shown (a) in Fig. 6.

[0058] If the horizontal blanking period is entered, $\phi Go=\phi T1$ gets "H", to write a signal o1A- of line memory 1 in the L1 row. Then, the vertical signal line is reset by a ϕc pulse, so that $\phi Ge=\phi T2$ gets "H", to write a signal o1B+ of line memory 2 in the row L2. Thereafter, the vertical signal line is reset to prepare for the signal writing at 2H. Similarly, at 2H, a signal o2A- is written in the row L3, and a signal o2B+ is written in the row L4. And at 3H, a signal o3A- is written in the row L5, but a signal o3B+ is not written in the row L6 because ϕGe remains "L".

[0059] At 4H, an image signal is written into the row L6 into which no signal is written at 3H. since the selection of row L6 is performed by a ϕGe pulse, the V3 pulse remains "H" at 4H, continuing from 3H. The row L6 is selected by ϕGe pulse, and the row L7 is selected by a ϕG pulse but not by a ϕGo. In this way, for every compression driving of image, the selection of row is switched by a drive pulse of the interlace circuit.

[0060] A vertical scan circuit of this example will be detailed below.

[0061] Fig. 7A is a partial circuit diagram of a bootstrap scan circuit in this example, and Fig.7B is a voltage waveform chart of each portion to present the operation of this example. The vertical scan circuit is of a. construction of having n unit circuits connected, in which a scan pulse $\phi 1$ to ϕn is sequentially output from each unit

circuit. Note that the potential of each portion in Fig. 7A is indicated such as V(1) using the number attached to each portion.

[0062] In the same figure, if a pulse $\phi v1$ rises in a state where a pulse Ps is applied in the unit circuit in Fig. 7A a transistor M1 conducts to cause the potential V(4) to increase. Since the potential V(4) is a gate potential of a transistor M2, the transistor M2 indicates a conductance corresponding to the potential V(4).

[0063] Subsequently, if the pulse $\phi v1$ falls and the pulse $\phi v2$ rises, the potential V(5) increases through the transistor M2. The increase in the potential V(5) is fed back to the gate of the transistor M2 through a capacitor C1, to cause the potential V(4) to increase due to a bootstrap effect. Since the increase in the potential V(4) acts to increase the conductance of transistor M2, the pulse $\phi v2$ passes without substantial voltage drop due to transistor M2 to cause the potential V(5) to increase through a transistor M3.

[0064] Since the potential V(5) is a gate potential of transistor M3, the conductance of transistor M3 rises correspondingly to the potential V(6).

[0065] Subsequently, if the pulse $\phi v1$ rises, the potential V(7) increases through a transistor M6. Owing to the bootstrap effect as above mentioned, the potential V(6) further increases along with the increase in the potential V(7). Since the increase in the potential V(6) acts to raise the conductance of transistor M5, the pulse $\phi v1$ causes the potential V(5) to increase through transistors M6 and M7 (see Fig. 7B). Accordingly, a transistor M10 indicates a conductance corresponding to the gate potential V(5).

[0066] Subsequently, if the pulse $\phi v2$ rises, the transistor M5 is turned on, so that the potential V(7) is reset to the ground potential, and the transistor M7 is turned off. Accordingly, the portion at potential V(8) is in floating condition.

[0067] At the same time, upon the pulse $\phi v2$ rising, the potential V(9) increases through the transistor M10. This potential increase causes the potential V(8) to further increase due to the bootstrap effect.

[0068] If such change in the potential V(8) is utilized as the scan pulse $\phi 1$, a high voltage scan pulse can be obtained.

[0069] Then, the potential V(8) is reset by the pulse $\phi v1$, and at the same time the potential V(12) increases, so that the potential further increase by a pulse that follows. This potential V(12) is utilized as the scan pulse $\phi 2$. Subsequently, likewise, high voltage scan pulses $\phi 3$ to ϕn are sequentially output in synchronization with the pulse $\phi v2$.

[0070] Note that if the timings for the drive pulses $\phi v1$ and $\phi v2$ are appropriately determined in Fig. 2, the waveform for the scan pulses $\phi 1$ to ϕn can be closer to the rectangle.

[0071] In order to cause the vertical scan circuit to output a long pulse, such as V(3) shown in Fig. 5A, the pulses such as $\phi v1$ and $\phi v2$ of Fig. 8 are input into the vertical scan circuit.

[0072] In this example, owing to delta arrangement of pixels, the sampling phases are out of phase by 180° as shown in (a) in Fig. 6.

[0073] In addition to the bootstrap scan circuit, a logic circuit with CMOS can be available.

(Example 2)

[0074] In the example 1, the image signal having different sampling phase and different signal polarity was written in field inversion into each row by two-row interpolation driving. On the other hand, in an example 2, a first image input circuit and a second image input circuit changes the sampling phase of image signal for every 1H. The display is a TFT type liquid crystal display as described in Fig. 1. The signal processing circuits 120-1, 120-2 of Fig. 2 are inverted for every 1H to output signals S1, S2 which are opposite in the signal polarity. Fig. 9 is a chart representing the sampling phase and the signal polarity correspondingly to each row. The meaning "A" and "B" and "+" and "-" is the same as in the example 1. If o1 signal is input in the odd field, A- signal is written in the row L1, and B+ signal is written in the row L2. If o2 signal is input, A- signal is written in the row L3 and B+ signal is written in the row L4. And if o3 signal is written, A- signal is only written in the row L5. The timing chart of this example is omitted, but ϕGo, ϕGe, ϕG, $\phi T1$, $\phi T2$, V1, V2,... are different from those of the example 1.

[0075] In this example, since the inversion operation which the signal processing circuits 120-1, 120-2 perform is to always invert the image signal for every 1H, the direct current potential control feedback time constant is smaller. Hence, the rising at the power on is faster, so that the integrating capacity can be reduced.

(Example 3)

[0076] An example 3 is one in which the signal polarity is inverted for every two rows on the display. The display is a TFT type liquid crystal display as in the example 1 and shown in Fig. 1. It is not necessary to change the phase in sampling because of the same sampling phase of input signal into the line memories 1, 2 as in the example 1. Fig. 10 is a chart representing the sampling phase and the signal polarity correspondingly to each row. The meaning "A" and "B" and "+" and "-" are the same as in the example 1. In the example 3, the signal polarity is basically inverted for every 1H, but when the image signal is compressed and written in one row, the inversion operation is temporarily stopped. In the odd field, when signal o3 is only written in the row L5, the inversion of signal o3 to be written from the line memory 2 is temporarily stopped. Also, when signal o7 is only written in the row L12, the inversion of signal o7 to be written from the line memory 1 is temporarily stopped. Thereby, because the positive polarity signal and the negative polarity signal are contained each in two rows,

whatever four rows in the panel is noted, the central voltage of inversion signal is not shifted.

(Example 4)

[0077] The number of rows for the display in an example 4 is the same as the number of scan lines for the NTSC signal, wherein the connection to each pixel occurs at every other row. The display is an active matrix type or a simple matrix type liquid crystal display. Fig. 11 represents a liquid crystal display of this example. Since the image signal is directly written in each row during the horizontal effective scan period, no line memory is necessary. Also in this example, there is an interlace circuits for the wirings of rows (L1, L2,...) identical to that of the example 1 as shown in Fig. 2. Fig. 12 is the timing chart of this example.

(Example 5)

[0078] In this example, a non-interlace conversion of writing 1H signal in two rows is performed, and data to be written in these two rows is sampled from the image signal individually. Therefore, it is possible to make sampling corresponding to the pixel array of liquid crystal panel. Also, by writing into and reading from the line memory asynchronously, that is, reading image signal data from the line memory while writing it into the same line memory, the line memory can be halved as compared with the synchronization method. It is noted that the vertical resolution can be improved by shifting the row of liquid crystal panel on which the image signal data is written during the same horizontal scan period by one row between the first field and the second field.

[0079] Fig. 13A shows the system configuration of a liquid crystal display unit in the present invention. 51 is an input terminal of image signal such as a television signal, 52 is a decoder for the conversion into RGB color signal, 53 is a line memory, 4 is an inversion control and signal amplification unit for sequentially switching the signal for every predetermined period in forward or reverse direction to provide an alternating current signal for the driving of the liquid crystal, and 5 is a logic unit for forming a pulse for the memory control, the inversion control and the driving of liquid crystal panel. 6 is a liquid crystal panel, of which 7 is a horizontal shift register (HSR) as scanning means in a horizontal direction, 8 is a vertical shift register (VSR) as scanning means in a vertical direction, and 9 is a pixel unit. An interlace signal input into terminal 51 is decoded by the decoder 52 and then converted into a line sequential scan signal in the line memory 53, so that the liquid crystal panel 6 is rewritten over its entire screen at a frequency of 60Hz (NTSC) or 50Hz (PAL).

[0080] Fig.14 shows a block diagram of a line memory unit. 1b,2b,3b are input image signals in the memory unit, 4b is a memory writing shift register (WSR), 26 is a start pulse (WST) for WSR, 27 is a clock pulse for WSR, 18b is a memory reading shift register (RSR), 28 is a start pulse (RST) for RSR, and 29 is a clock pulse for RSR. 19b,20b,21b are output lines for image signal data.

[0081] Fig. 15 shows a color array of pixel. The pixel arrangement is in a mosaic type delta array. Therefore, different color pixels are connected to the vertical signal line (15 in Fig. 13B). Also, the pixel position in the horizontal direction is shifted by 0.5 pixel, or 1.5 pixels for the same color pixel, between the even row and the odd row.

[0082] Fig.13B shows the circuit configuration of a display unit in the liquid crystal panel. 7 is a horizontal shift register (HSR), 8 is a vertical shift register (VSR), and 9 is a pixel unit. 10 is a thin film transistor, 11 is a liquid crystal, 12 is a holding capacitor, 13 is an opposed electrode, 14 is an image signal input line, 15 is a vertical signal line, 16 is a gate line, and 17 is a signal line select switch. 72 is a clock pulse for HSR, and 82 is a clock pulse for VSR.

[0083] Fig. 16 is a chart showing the operation timing for the line memory unit and the liquid crystal panel unit, wherein SIG1 is an input image signal (R, G, B) for the memory unit, SIG2 is a start pulse of the memory writing shift register (WSR), SIG3 is a WSR clock pulse, SIG4 is a start pulse of the memory reading shift register (RSR), and SIG5 is a clock pulse for RSR. SIG6 is a signal (ODD) indicating whether the row number is odd or even, SIG7 is a start pulse of the horizontal shift register (HSR) for the liquid crystal panel, and SIG8 is a clock pulse for HSR.

[0084] Referring to Fig. 14 there is described in this example an instance of displaying on the liquid crystal having a horizontal pixel number of 600, a vertical pixel number of 480. The image signals of this example is sampled from right to left. The image signals 1b,2b 3b which have been subjected to gamma correction suitable for the liquid crystal display in the decoder unit at the former stage and intermediate amplification in accordance with the dynamic range of line memory are sampled by the shift register 4 having 2 x 600 stages, and written into the line memory 30 through the transistors 5b, 6b, 7b . The sampling is performed 1200 times which is twice a horizontal pixel number of the liquid crystal panel during one horizontal period. The sampling is performed in the order of R, G, B in accordance with the liquid crystal panel, and the signal is written into the line memory in the order of Ro1, Ge1, Bo1, Re1, Gol, Be1, ... (Roi, Goi, Boi represent data corresponding to the even row of liquid crystal panel, Rei, Gei, Bei represent data corresponding to the odd row of liquid crystal panel).

[0085] On the other hand, the reading of data from the line memory is performed separately for the even row data of liquid crystal panel Ro1, Go1, Bo1, Ro2, Go2, ... Ro200, Go200, Bo200, and the odd row data Re1, Ge1, Be1, Re2, Ge2, ... Re200, Ge200, Be200, both being transferred to the liquid crystal panel during one horizontal scan period. Since at the time of sampling, the

phase is shifted by the amount corresponding to one pixel of liquid crystal panel between Roi, Goi and Boi, and between Rei, Gei and Bei, the reading from the line memory and the writing into the liquid crystal panel are performed at the same time for the above three pixels. That is, when data at the first row is transferred to the liquid crystal panel, the transistors 12b,13b,14b conduct, because an AND gate 10b gets "H" if an ODD signal 9b gets "H", the output at the first stage of the shift register 18b gets "H", so that data Rol, Gol, Bol are output to the output signal lines 19b,20b,21b at the same time. Similarly, when data at the second row is transferred to the liquid crystal panel, the transistors 15b,16b, 17b conduct, because an AND gate 11b gets "H" if ODD signal 9b gets "H" and the output at the first stage of the shift register 18b gets "H", so that data Re1, Ge1, Be1 are output to the output signal lines 19b,20b,21b at the same time.

[0086] The writing into and the reading from the line memory are performed in the following order. First, upon a start signal 26 of the shift register4b at the writing side, the shift register 4b starts the operation, making sampling 1200 times during one horizontal scan period, and sequentially writing into the line memory. At the time when the sampling (600+6) times or more is ended, upon a start signal 28 of the shift register 18b at the reading side, the operation of the shift register 18b if started, so that data at the odd address is read in the order of 1, 3, 5 addresses (Ro1, Go1, Bo1), and 7, 9, 11 addresses (Ro2, Go2, Bo2) of the line memory, three data at the same time. If the frequency of read clock at this time is three times that of the write clock, the reading up to the (1200-6)-th address has been performed at the time when the writing into the line memory is ended, whereby the reading is not performed before the writing into the line memory. Also, the reading is performed within $t_H/2$ which is half one horizontal scan period t_H, while the writing into the first row of the liquid crystal panel is ended. During the next $t_H/2$ period, data at the even address is read, three data at the same time, in the order of 2, 4, 6 addresses (Be1, Re1, Ge1), 8, 10, 12 addresses (Be2, Re2, Ge2), ... in the same manner as above described. Then, the sampling of image signal for the next horizontal scan period is performed, and data is written into the line memory, but the order of the writing and reading is not reversed if the reading precedes the writing.

[0087] Where the reading of data is performed after the end of the writing into the line memory, a line memory for the image signal during two horizontal scan periods is required, but by reading the image signal data from the line memory while writing into the same line memory, as in this example, the line memory can be halved.

[0088] The above timing is shown in Fig. 16. The read data is converted into an alternating signal by an inversion amplifier 4 of Fig. 13A, and input into the liquid crystal panel 6. The horizontal shift register 7 of this liquid crystal panel has the same stage number as the shift register (18b in Fig. 14) in the line memory unit, and is driven at the same timing. Also, the vertical shift register 8 of 480 stages performs the shift operation prior to a reading start signal in the line memory unit.

[0089] By repeating the above operation during 240 horizontal scan periods, the image signal data can be written into the 480 rows in the liquid crystal panel for one field. Note that the row of the liquid crystal panel on which the image signal data is written during the same horizontal scan period may be the same or shifted by one row as shown in Fig. 17, between the first field and the second field, but when shifted by one row, the vertical resolution can be improved. Fig. 17 shows the signal to be written onto each row from 2k to 2(k+1) for every field.

[0090] Herein, Ok and O'k are data in the first field (odd field), and Ek and E'k data in the second field (even field), which is obtained by sampling the image signal during the k-th horizontal scan period for the interlace signal, in accordance with the pixel array in the odd row and the even row of the liquid crystal panel and at different timings. In this case, the start timing of the vertical shift register in the second field occurs $t_H/2$ ahead of the first field, and the reading order of the line memory occurs from the odd row data (Be1, Re1, Ge1, ...).

[0091] The liquid crystal panel has different color pixels connected to the vertical signal line, but another example is a liquid crystal panel in which the same color pixels are connected to the vertical signal line as shown in Fig. 19 in which case the wiring on the reading side of the line memory should be made as shown in Fig. 18.

[0092] While in this example, a capacitor is used as holding means of image signal which is held in the state of analog signal (memory unit 53 in Fig. 13A), this portion may be constituted of an A/D converter, a digital line memory, and a D/A converter.

[0093] And by providing driving means as previously described, the image signal of various standards can be displayed.

[0094] The horizontal pixel array of adjacent two lines is shifted by 0.5 pixel, and the color pixel of R, G, and B is arranged in delta configuration, whereby a smooth display with high horizontal resolution can be effected.

[0095] Also, by reading the image signal data from the line memory while writing into the same line memory, the line memory can be halved as compared with when the data is read after the end of writing into the line memory.

[0096] Further, by shifting the row of liquid crystal panel on which the image signal data is written during the same horizontal scan period between the first field and the second field, by one row, the vertical resolution can be improved.

(Example 6)

[0097] This example is configured to rewrite the entire screen at every 60Hz, by serially inputting the signal, forming two kinds of signals sampled at different timings

from the same horizontal scan signal, using an analog line memory capable of serially outputting data in different order and at different frequency when reading than when inputting, and writing them into two pixel rows during one horizontal scan period, while shifting one row the combination of two rows to scan in the even field and the odd field. Thereby, in the low cost, smaller systems, it is possible to realize the good image quality with high resolution and high gradation, and without flicker, and readily form special reproduction image such as enlargement and reduction of screen in the horizontal direction, or left and right inversion of screen, with less wirings.

[0098] Fig. 15 shows a color array of pixels in the liquid crystal panel for use in this example. Herein, the circuit configuration of a display unit for the liquid crystal panel is as shown in Fig. 13B and the pixel arrangement is in a mosaic type delta array. Therefore, different color pixels are connected to vertical signallines 15 of Fig. 13B. Also, the position of the same color pixel in the horizontal direction is shifted by one half period (1.5 pixels) between the even row and the odd row, the timing for each color signal is changed for the sampling between the even row and the odd row.

[0099] In Fig. 13A the system configuration for a liquid crystal display using a line memory which implements the serial IN - serial OUT employing row types of shift registers for reading and writing is shown. 51 is an output terminal for TV signal, 52 is a decoder unit for converting composite TV signal into RGB color signal 53 is an analog line memory unit, 4 is an inversion control and signal amplification unit for sequentially switching the signal for every predetermined period in forward and reverse direction to provide a signal for the driving of liquid crystal, and 5 is a logic unit for forming a pulse for the memory control, the inversion control and the driving of liquid crystal panel. 6 is a liquid crystal panel, of which 7 is a horizontal shift register (HSR) as scanning means in the horizontal direction, 8 is a vertical shift register (VSR) as scanning means in the vertical direction, and 9 is a pixel unit. An interlace signal input at 51 is color decoded at 52, and then converted into line sequential scan signal by the line memory at 53 so that the liquid crystal panel at 6 is rewritten on its entire screen at 60Hz period. Herein, the signal information is sampled according to a spatial arrangement of R, G and B pixels and is written into the memory 53. Besides it is possible that the RGB signal is subjected to a different amount of delay in accordance with the order of pixel array for RGB in the decoder unit 52. In this case, the signal information can be obtained in accordance with the spatial arrangement of pixels on the liquid crystal at the same sampling pulse, whereby the frequency of sampling clock for the memory unit and the liquid crystal panel is made one-third.

[0100] Fig. 20 shows a block diagram of the analog line memory unit in this example. 318 is an input stage of the memory unit, 319 is a memory writing shift register (WSR), 320 is a WSR start pulse (WST), 321-1, 321-2 are WSR two-phase clock pulses (WCLK1, WCLK2), 322 is a memory reading shift register (RSR) 323 is an RSR start pulse (RST), and 324 is an RSR clock pulse (RCLK). 325 is switching control unit for switching the signal to be sent to the video line in accordance with the color array for the liquid crystal panel. 33 is a sample and hold circuit, and 34 is an input terminal of sample and hold pulse. 326 is an output stage of the memory unit. 327R,327G,327B are input terminals for RGB signals, 328A, 328B,328C are output terminals for outputting data through the switching by switches at 325 between the even row and the odd row of the liquid crystal screen for writing R and G, G and B, B and R, in which 329 is an input terminal of the switching control signal. 35 is a control terminal of the switching control signal. 35 is a control terminal for fine regulating the reading timing from the memory, its role being described later. 30a to 30f are memory arrays for the even row and the odd row of the liquid crystal screen of each color of RGB, which are allocated from the same horizontal signal alternately at every other clock for the shift register for writing. A specific constitutional example of this portion is shown in Fig. 27. Herein, 43A, 43B, 43C indicates the output line of memory between 325 and 33 in Fig. 20. Also, 1 to n of 30a to 30f represents 1 bit to n bit of the memory array, respectively. When the signal is read, 30a, 30c, 30e or 30b, 30d, 30f is selected by a switching control signal at 329.

[0101] Fig. 21 shows the liquid crystal and memory driving timing in the horizontal scan period. SG1R is a red image signal, SG1G is a green image signal, SG1B is a blue image signal, SG2 is WST, SG3 is WCLK1, SG4 is WCLK2, SG5 is RST, SG6 is RCLK, SG7 is a color select switching signal, SG8A to C are signals converted into the line sequential scan signal which is output from the memory unit, SG9 is HST, SG10 is H1, and SG11 is H2.

[0102] By taking such configuration, the serial signal sampled at double density is taken out at every other time, then modified to two serial signals of which the order is changed to conform to the pixel arrangement of the liquid crystal screen, and scanned continuously during one horizontal scan period by the reading shift register operating at another clock, while being switched to each output terminal.

[0103] Fig. 22 shows the signals to be written into each row (2n to 2(n+2)) for every field on the liquid crystal panel in this example. Herein, $O_n(m)$ and O_n. (m) are data which is obtained by sampling the n-th signal in the odd row for the interlace signal in the m-th frame at different timings in accordance with the pixel array of the even row and the odd row for the panel.

[0104] Since both the even row and the odd row on the screen is rewritten at every one field (60Hz), the problem with the varying resolution and flicker can be resolved. Also, observing one field, the resolution in the vertical direction is halved from that of the original sig-

nal, but by shifting one row in the next field for the display, the vertical resolution is raised artificially.

[0105] In this way, in the line memory with low cost, the interlace signal is converted into the line sequential scan signal to realize the excellent image quality.

[0106] By the way, the serial signal sampled at double density herein is modified to two serial signals of which the order is changed to conform to the pixel arrangement of the liquid crystal screen, but when the color array order for the even row and the odd row is the same such as an inline-type pixel array, the interlace signal is converted into the line sequential scan signal to have effect of realizing the excellent image quality, in the line memory with low cost, without changing the order of sampled signals, depending on the relation between pixel array and memory array.

[0107] Herein, in order to explain the role of a fine regulation switch for the memory reading position 35 in Fig. 20, the memory output signal and the signal to be written into the pixel of liquid crystal panel are considered. Fig. 23 represents each signal of the memory unit in Fig. 21. SG21 is a memory reading start pulse, and SG22 is a reading clock. SG23 is a memory output before the sample and hold. SG24 is a sample and hold pulse for sampling SG23 when rising and holding it when falling. SG25 is an output signal after the sample and hold.

[0108] In this way, the signal read from the memory is input via an inversion control amplifier into a video signal input terminal 14 for the liquid crystal panel in Fig. 14B, and by applying a sequential voltage to the gate of a vertical signal line select transistor 17 by means of a horizontal shift register 7, the liquid crystal of pixel selected in a thin film transistor 10a and the holding capacitor are charged sequentially. The behavior of charging at this time is shown in Fig. 25. SG26 and SG27 are gate voltages for the vertical signal line select transistors 14a adjacent to each other, SG28, SG29 are the potential change in the liquid crystal and the holding capacitor of adjacent pixels connected to respective vertical signal lines and selected by corresponding thin film transistor 10a.

[0109] However, because each bit output from the memory of SG25 and the vertical signal select signal of SG26, SG27 are out of phase in the example of Fig. 14, the select period extends over the next bit. Therefore, the charging potential of pixel becomes a potential determined by the next bit in the final select period, though the intrinsic bits are charged. As a result, the intrinsic signal is not displayed on the liquid crystal panel. In particular, where the delay time of select panel or the delay time of signal is different depending on the liquid crystal panel, it is necessary to adjust the memory output to the optimal phase relation if the same memory is utilized.

[0110] Herein, as an example, using a circuit as shown in Fig. 25, the memory reading clock is shifted by one-half phase with respect to the memory start pulse in accordance with the switch control at 35 in Fig. 20. The memory reading clock (R CLK) inputted from a terminal 324is applied to terminal 37. From a terminal 38, a reading clock with a phase controller is outputted. At this time, each signal and the charging potential of pixel are shown in Fig. 26. Because the memory reading clock is shifted by one-half phase with respect to the start pulse, the output of each bit from the memory SG25 and the vertical signal line select signal of SG26, SG26 are in phase with each other, so that the intrinsic signal is charged in the liquid crystal pixel. Of course, by providing the terminal for fine regulation at 35 with more bits, the finer phase regulation is enabled, resulting in extended utilization of memory and better image quality.

[0111] And by driving means as previously described, the image signal of various standards can be displayed.

(Example 7)

[0112] Fig. 28 shows a block diagram of an analog line memory unit for implementing the serial IN - serial OUT equipped with a writing shift register and a reading X-directional scan decoder as the example 7. The overall system has the same configuration as shown in Fig. 13A In Fig. 28, 318 is an input stage of the memory unit, 319 is a memory writing shift register (WSR), 320 is a WSR start pulse (WST), 321-1,321-2 are WSR two-phase clock pulses (WCLK1, WCLK2), 36 is a memory reading decoder (RDECO), 31 is a control unit for controlling the decoder, and 32 is a path through which the control signal is transferred from the control unit. 325 is a switching control unit for switching the signal to be sent to the video line in accordance with the color array for the liquid crystal panel. 326 is an output stage of the memory unit. 327R, 327G, 327B are input terminals for RGB signals, respectively, 328A, 328B, 328C are output terminals for outputting data through the switching by switches at 325 between the even row and the odd row of the liquid crystal screen for writing R and G, G and B, B and R, in which 329 is an input terminal of the switching control signal. 30a to 30f are memory arrays for the even row and the odd row of the liquid crystal screen for each color of RGB.

[0113] Fig. 29 shows the liquid crystal and memory driving timing in the horizontal scan period in this example. SG1R is a red image signal, SG1G is a green image signal, SG1B is a blue image signal, SG2 is WST, SG3 is WCLK1, SG4 is WCLK2, SG7 is a color select switching signal, SG8A to C are signals converted into the line sequential scan signal which is output from the memory unit in accordance with the control signal of decoder, wherein by reading a part ("a" portion) of the signal in the horizontal scan period stored in the memory, the screen is enlarged in the horizontal direction. SG9 is HST, SG10 is H1, and SG11 is H2. Herein, the X decoder control pulse is omitted.

[0114] Figs. 30A and 30B show typical views in which Fig. 30A is an original image and Fig. 30B is an image realized by this example.

[0115] As in this example, by changing the order of

memory reading means and memory writing means, or using a line memory having a constitution of changing the operation frequency or start position of the shift register, the special image display such as enlargement or reduction of the screen, left and right inversion of screen, screen movement, in the horizontal direction, can be realized even with the system of line memory at low cost and with simple constitution.

[0116] And the image signal of various standards can be displayed by driving means as previously described.

(Example 8)

[0117] An example 8 is one in which the present invention is applied to an electron beam flat display. The display is a flat panel in which each pixel has an electron source and a fluorescent screen which is excited for radiation by electrons outgoing from the electron source. Fig. 31 represents simply its electron beam flat display. In the figure, 105 is a rear plate, 106 is a screen, 107 is a face plate, which constitutes an airtight Container, thereby maintaining the interior of the container in vacuum. 101 is a substrate, 102 is an electron beam, 103 is a wiring in the row direction, 104 is a wiring in the column direction, which are secured to the rear plate 105. 108 is a fluorescent body, and 109 is a metal back, which are secured to the face plate 107. The electron source 102 excites the fluorescent body 108 for radiation by causing electrons to impinge against the fluorescent body 108. The fluorescent body is disposed which can emit three primary colors of red, blue and green. The metal back 109 secularly reflects back the light which the fluorescent body 108 emits to enhance the light utilization efficiency, thereby protecting the fluorescent body 108 from the electron impingement, and fulfilling a role of accelerating electrons by high voltage from a high voltage input terminal Hv. The electron source 102 is composed of M sources longitudinally arranged and N sources transversely arranged, and a total of MxN sources, which are connected through M wirings 103 in the low direction and N wirings 104 in the column direction, these wirings being orthogonal to one another. Dx1, Dx2, ... DxM are input ends for the wirings in the row direction, and Dy1, Dy2, ... DyN are input ends for the wirings in the column direction. The wirings 103 in the row direction are data wirings, and the wirings in the column direction 104 are scan wirings.

[0118] With such an electron beam flat display, the image signal of standards can be displayed by using vertical scan altering means as previously described.

[0119] In this example, the image signal of various standards is inversely input to the panel, while the distortion of image can be reduced to the utmost.

Claims

1. A method of driving a colour display panel (20,6) having pixels (10) arranged in m rows (L1-Lm) and n columns (D1-Dn) in an RGB colour coded delta formation, to display an image represented by an image signal determined for k effective raster scan lines (o1-ok, el-ek) for each odd and even image field (o,e), which method includes normal mode operation steps of performing two-row interpolation driving whereby writing of image line data obtained from said image signal is enabled line sequentially, and in-phase and anti-phase sample image line data (A,B), for a corresponding image scan line are written on respective ones of two consecutive matrix rows (L1 & L2, L3 & L4, ...) during each horizontal scan period (1H, 2H, ..) in an alternating order (A,B,A,B), the polarities of the line data (A,B) written to each matrix row alternating from one matrix row (L1, L3, ...) to the next matrix row (L2,L4,...) or from one pair of matrix rows (L1 & L2, L5 & L6, ...) to the next pair of matrix rows (L3 & L4, L7 & L6, ...);

   characterised in that:

   to display an image wherefor the number k of scan lines is different from m and different from m/2, and has a value therebetween, said method is modified by compression mode operation steps which all are performed repeatedly after respective numbers of horizontal scan periods (2H,6H,...3H,7H...), said compression mode operation steps consisting in:

      interrupting said two-row interpolation driving following the writing of the first one of said in-phase or anti-phase sample image line data (A,B) to the first of the two consecutive matrix rows written in the following horizontal scan period (3H,7H,...,4H,7H);
      suppressing the writing of the second one of said in-phase or anti-phase sample image line data (A,B) that would be written to the second of said two consecutive matrix rows; and
      resuming said two-row interpolation driving for the next following horizontal scan period (4H,8H,...5H,9H) starting with writing to said second of said two consecutive rows, in which the alternating order (A,B,A,B) of writing said in-phase and anti-phase sample image line data is reversed (B,A,B,A,..) and the sequence of alternating polarity of the written image signals is maintained without disruption.

2. A method according to claim 1 wherein said in-phase and anti-phase sample image line data are written with one and the opposite polarity in each odd field and the inverse of said one and the opposite polarity in each even field.

3. A method according to claim 1 wherein, during said two-row interpolation driving, said in-phase and anti-phase sample image line data are written with polarities that are inverted for each alternate horizontal scan period, which in-phase and anti-phase sample image line data written in respective horizontal scan periods have the respective same polarity (A^+ & B^+, A^- & B^-) when written in said alternating order (A,B,A,B) and have respective opposite polarity (A^- & B^+, A^+ & B^-) when written in the reversed alternating order (B,A,B,A,...).

4. A method according to any of claims 1 to 3 applied to an active matrix liquid crystal colour display panel (6:fig.14).

5. A method according to any of claims 1 to 3 applied to an electron-emitting colour display panel (101-109) comprising a colour-coded fluorescent body (108) and an electron source (101-104), having an electron-emitting device (102) for each of said pixels, arranged opposite to said fluorescent body.

6. A colour display apparatus operable according to the method of claim 1 comprising:

a colour display panel (6,20) having pixels (10) arranged in m rows (L1-Lm) and n columns (D1-Dn) in an RGB colour coded delta formation, to display an image represented by an image signal having k effective raster scan lines (o1-ok, e1-ek) for each odd and even image field (o,e); and
driving means for driving said display panel in a two-row interpolation manner, said driving means including:

writing means (80-1, 80-2, 100-1, 100-2, 120-1, 120-2) for writing paired in-phase and anti-phase sample image line data (A, B), each pair corresponding to respective scan lines of the image represented by the image signal, on respective pairs of first and second consecutive matrix rows, the polarities of the line data (A,B) to be written to each matrix row alternating from one matrix row (L1, L3,...) to the next matrix row (L2,L4,...) or from one pair of consecutive matrix rows (L:1 & L2, L5 & L6,...) to the next pair of consecutive matrix rows (L3 & L4, L7 & L8,...);
selecting means (40,60,..1-1 to 1-3, 2-1 to 2-3) for selecting said matrix rows line sequentially for writing said line data, two-consecutive matrix rows at consecutive times in each horizontal scan period; and
control means (140) arranged to control said writing means and said selecting means, to control the relative timing and sequence of the operation thereof;

characterised in that:

to display an image wherefor the number k of scan lines is different from n and different from m/2, and has a value therebetween, said driving means is adapted to perform said compression mode operation steps and thus includes:

means of interrupting two-row interpolation driving;
means of suppressing said writing of the second one of in-phase and anti-phase sample image line data; and
means of resuming said two-row interpolation driving.

7. Apparatus according to claim 6 wherein
said selection means (40,60;...1-1 to 1-3, 2-1 to 2-3) includes:

a first array of switches (1-1 to 1-3,..) connected between odd matrix rows (L1,L3,L5,...) of the display panel and a first control line for inputting a first scan voltage signal (ΦG_o);
a second array of switches (2-1 to 2-3...) connected between even matrix rows (L2,L4,L6,...) of the display panel and a second control line for inputting a second scan voltage signal (ΦG_o);
a third array of switches (3-1 to 3-3,...) connected between the third and subsequent odd matrix rows (L3,L5,L7,...) of the display panel and a third control line for inputting a third scan voltage signal (ΦG); and
a gating signal generating means (40) for generating respective sequential gating signals (V1,V2,V3,...) and supplying each to a respective group of three switches, one switch (1-1,2-1 & 3-1; 1-2,2-2,3-2,...) in each first, second and third array;
said control means supplies said first to third scan voltage signals (ΦG_o,ΦG_e,ΦG), which signals (ΦG_o,ΦG_e) gated by said switches of said first and second arrays are to enable two-row interpolation driving in said alternating order,
which signals (ΦG_e,ΦG) gated by said switches of said second and third arrays are to enable two-row interpolation driving in said reverse alternating order, and
which signals (ΦG_e,ΦG) respectively gated by said switches of said second and third arrays are to suppress writing following interruption of said two-row interpolation driving in said alter-

nating order and in said reverse alternating order, respectively; and
said control means is arranged to control said gating signal generating means to generate and supply modified gating signals (V3,...) to facilitate writing, starting from the second of two consecutive rows, each time two-row interpolation driving is resumed.

8. Apparatus according to claim 7 wherein said writing means includes respective line memories (100-1,100-2) for storing the in-phase and anti-phase sample image line data that is to be used in writing to the display panel.

9. Apparatus according to any of claims 6 to 8 wherein said colour display panel (20) is an active matrix liquid crystal display panel (6:fig.14).

10. Apparatus according to any of claims 6 to 8 wherein said colour display panel (20) is an electron-emitting colour display panel (101-109) comprising a colour-coded fluorescent body (108) and an electron source (101-104) having an electron-emitting device (102) for each of said pixels, arranged opposite to said fluorescent body.

Patentansprüche

1. Verfahren zum Ansteuern eines Farbanzeigefelds (20, 6) mit Pixeln (10), die in m Reihen (L1-Lm) und n Spalten (D1-Dn) in einer RGB-farbcodierten Deltaformation angeordnet sind, zum Anzeigen eines Bilds, das durch ein für k effektive Rasterabtastzeilen (o1-ok, e1-ek) für jedes ungerade und gerade Bildfeld (o, e) bestimmtes Bildsignal repräsentiert wird, welches Verfahren Normalbetriebsablaufschritte zum Durchführen einer Zweireihen-Interpolationsansteuerung beinhaltet, wodurch ein Schreiben von aus dem Bildsignal erhaltenen Bildzeilendaten zeilensequentiell ermöglicht wird und inphasige und gegenphasige Abtastbildzeilendaten (A, B) für eine entsprechende Bildabtastzeile in jeweilige zweier aufeinanderfolgender Matrixreihen (L1 & L2, L3 & L4, ...) während jeder horizontalen Abtastperiode (1H, 2H, ..) in alternierender Reihenfolge (A, B, A, B) geschrieben werden, wobei die Polaritäten der Zeilendaten (A, B), die in jede Matrixreihe geschrieben werden, von einer Matrixreihe (L1, L3, ...) zu der nächsten Matrixreihe (L2, L4, ...) oder von einem Paar von Matrixreihen (L1 & L2, L5 & L6, ...) zu dem nächsten Paar von Matrixreihen (L3 & L4, L7 & L6, ...) alternieren;
dadurch gekennzeichnet, daß:

zum Anzeigen eines Bilds, für welches die Zahl k von Abtastzeilen von m verschieden ist und von m/2 verschieden ist, und einen Wert zwischen diesen hat, das Verfahren durch Kompressionsbetriebsablaufschritte modifiziert wird, welche nach jeweiligen Anzahlen horizontaler Abtastperioden (2H, 6H, ..., 3H, 7H, ...) alle wiederholt durchgeführt werden, wobei die Kompressionsbetriebsablaufschritte bestehen im:

Unterbrechen der Zweireihen-Interpolationsansteuerung folgend auf das Schreiben der ersten der inphasigen oder gegenphasigen Abtastbildzeilendaten (A, B) in die erste der beiden aufeinanderfolgenden Matrixreihen, die in der folgenden horizontalen Abtastperiode (3H, 7H, ..., 4H, 7H) geschrieben werden;
Unterdrücken des Schreibens der zweiten der inphasigen oder gegenphasigen Abtastbildzeilendaten (A, B), die in die zweite der beiden aufeinanderfolgenden Matrixreihen geschrieben werden würden; und
Wiederaufnehmen der Zweireihen-Interpolationsansteuerung für die nächste folgende horizontale Abtastperiode (4H, 8H, ..., 5H, 9H) beginnend mit dem Schreiben in die zweite der beiden aufeinanderfolgenden Reihen, wobei die alternierende Reihenfolge (A, B, A, B) des Schreibens der inphasigen und gegenphasigen Abtastbildzeilendaten umgekehrt wird (B, A, B, A) und die Abfolge alternierender Polarität der geschriebenen Bildsignale ohne Unterbrechung aufrechterhalten wird.

2. Verfahren nach Anspruch 1, bei dem die inphasigen und gegenphasigen Abtastbildzeilendaten mit einer und der dazu entgegengesetzten Polarität in jedes ungerade Feld und das Inverse der einen und der dazu entgegengesetzten Polarität in jedes gerade Feld geschrieben werden.

3. Verfahren nach Anspruch 1, bei dem während der Zweireihen-Interpolationsansteuerung die inphasigen und die gegenphasigen Abtastbildzeilendaten mit Polaritäten geschrieben werden, die für jede zweite horizontale Abtastperiode invertiert sind, welche inphasigen und gegenphasigen Abtastbildzeilendaten, die in jeweiligen horizontalen Abtastperioden geschrieben werden, die jeweils gleiche Polarität (A^+ & B^+, A^- & B^-) haben, wenn sie in der alternierenden Reihenfolge (A, B, A, B) geschrieben werden, und jeweils entgegengesetzte Polarität (A^- & B^+, A^+ & B^-) haben, wenn sie in der umgekehrten alternierenden Reihenfolge (B, A, B, A, ...) geschrieben werden.

4. Verfahren nach einem der Ansprüche 1 bis 3, an-

gewandt auf ein Aktivmatrix-Flüssigkristall-Farbanzeigefeld (6: Fig. 14).

5. Verfahren nach einem der Ansprüche 1 bis 3, angewandt auf ein Elektronen emittierendes Farbanzeigefeld (101-109) mit einem farbcodierten fluoreszierenden Körper (108) und einer dem fluoreszierenden Körper gegenüberliegend angeordneten Elektronenquelle (101-104) mit einer Elektronen emittierenden Einrichtung (102) für jedes der Pixel.

6. Farbanzeigevorrichtung, betreibbar in Übereinstimmung mit dem Verfahren nach Anspruch 1, umfassend:

ein Farbanzeigefeld (6, 20) mit Pixeln (10), die in m Reihen (L1-Lm) und n Spalten (D1-Dn) in einer RGB-farbcodierten Deltaformation angeordnet sind, zum Anzeigen eines Bilds, das durch ein Bildsignal mit k effektiven Rasterabtastzeilen (o1-ok, e1-ek) für jedes ungerade und gerade Bildfeld (o, e) repräsentiert wird; und

eine Ansteuereinrichtung zum Ansteuern des Anzeigefelds nach dem Prinzip einer Zweireihen-Interpolation, wobei die Ansteuereinrichtung einschließt:

eine Schreibeinrichtung (80-1, 80-2, 100-1, 100-2, 120-1, 120-2) zum Schreiben gepaarter inphasiger und gegenphasiger Abtastbildzeilendaten (A, B), wobei jedes Paar jeweiligen Abtastzeilen des durch das Bildsignal repräsentierten Bilds entspricht, in jeweilige Paare erster und zweiter aufeinanderfolgender Matrixreihen, wobei die Polaritäten der in jede Matrixreihe zu schreibenden Zeilendaten (A, B) von einer Matrixreihe (L1, L3, ...) zu der nächsten Matrixreihe (L2, L4, ...) oder von einem Paar aufeinanderfolgender Matrixreihen (L1 & L2, L5 & L6, ...) zu dem nächsten Paar aufeinanderfolgender Matrixreihen (L3 & L4, L7 & L8, ...) alternieren;

eine Auswahleinrichtung (40, 60, ..., 1-1 bis 1-3, 2-1 bis 2-3) zum zeilensequentiellen Auswählen der Matrixreihen zum Schreiben der Zeilendaten, zwei aufeinanderfolgende Matrixreihen zu aufeinanderfolgenden Zeiten in jeder horizontalen Abtastperiode; und

eine Steuereinrichtung (140), die zum Steuern der Schreibeinrichtung und der Auswahleinrichtung angeordnet ist, um das relative Zeitverhalten und die Abfolge des Betriebsablaufs derselben zu steuern;

dadurch gekennzeichnet, daß:

zum Anzeigen eines Bilds, für welches die Zahl k von Abtastzeilen von m verschieden ist und von m/2 verschieden ist, und einen Wert zwischen diesen hat, die Ansteuereinrichtung dazu ausgelegt ist, die Kompressionsbetriebsablaufschritte durchzuführen, und somit einschließt:

eine Einrichtung zum Unterbrechen der Zweireihen-Interpolationsansteuerung;

eine Einrichtung zum Unterdrücken des Schreibens der zweiten von inphasigen oder gegenphasigen Abtastbildzeilendaten; und

eine Einrichtung zum Wiederaufnehmen der Zweireihen-Interpolationsansteuerung.

7. Vorrichtung nach Anspruch 6, bei der die Auswahleinrichtung (40, 60; ... 1-1 bis 1-3, 2-1 bis 2-3) einschließt:

ein erstes Feld von Schaltern (1-1 bis 1-3, ..), die zwischen ungeraden Matrixreihen (L1, L3, L5, ...) des Anzeigefelds und einer ersten Steuerleitung zum Zuführen eines ersten Abtastspannungssignals (ΦG_0) verschaltet sind;

ein zweites Feld von Schaltern (2-1 bis 2-3, ...), die zwischen geraden Matrixreihen (L2, L4, L6, ...) des Anzeigefelds und einer zweiten Steuerleitung zum Zuführen eines zweiten Abtastspannungssignals (ΦG_0) verschaltet sind;

ein drittes Feld von Schaltern (3-1 bis 3-3, ...), die zwischen der dritten und nachfolgenden ungeraden Matrixreihen (L3, L5, L7,...) des Anzeigefelds und einer dritten Steuerleitung zum Zuführen eines dritten Abtastspannungssignals (ΦG) verschaltet sind; und

eine Torsignal-Erzeugungseinrichtung (40) zum Erzeugen jeweiliger sequentieller Torsignale (V1, V2, V3, ...) und Zuführen jedes derselben zu einer jeweiligen Gruppe von drei Schaltern, einem Schalter (1-1, 2-1 & 3-1; 1-2, 2-2 & 3-2, ...) in jedem ersten, zweiten und dritten Feld; wobei

die Steuereinrichtung die ersten bis dritten Abtastspannungssignale (ΦG_o, ΦG_e, ΦG) zuführt, welche Signale (ΦG_o, ΦG_e), die durch die Schalter des ersten und des zweiten Felds geschleust werden, dazu dienen, die Zweireihen-Interpolationsansteuerung in der alternierenden Reihenfolge zu ermöglichen,

welche Signale (ΦG_e, ΦG), die durch die Schalter des zweiten und des dritten Felds geschleust werden, dazu dienen, die Zweireihen-Interpolationsansteuerung in der umgekehrten alternierenden Reihenfolge zu ermöglichen,

welche Signale (ΦG_e, ΦG), die jeweils durch

die Schalter des zweiten und des dritten Felds geschleust werden, dazu dienen, ein auf die Unterbrechung der Zweireihen-Interpolationsansteuerung in der alternierenden Reihenfolge bzw. in der umgekehrten alternierenden Reihenfolge folgendes Schreiben zu unterdrükken; und

die Steuereinrichtung so angeordnet ist, daß sie die Torsignal-Erzeugungseinrichtung zum Erzeugen und Liefern modifizierter Torsignale (V3, ...) steuert, um das Schreiben zu erleichtern, beginnend bei der zweiten zweier aufeinanderfolgender Reihen, jedesmal dann, wenn die Zweireihen-Interpolationsansteuerung wieder aufgenommen wird.

8. Vorrichtung nach Anspruch 7, bei der die Schreibeinrichtung jeweilige Zeilenspeicher (100-1, 100-2) einschließt zum Speichern der inphasigen und gegenphasigen Abtastbildzeilendaten, die bei dem Schreiben auf das Anzeigefeld zu verwenden sind.

9. Vorrichtung nach einem der Ansprüche 6 bis 8, bei der das Farbanzeigefeld (20) ein Aktivmatrix-Flüssigkristall-Anzeigefeld (6: Fig. 14) ist.

10. Vorrichtung nach einem der Ansprüche 6 bis 8, bei der das Farbanzeigefeld (20) ein Elektronen emittierendes Farbanzeigefeld (101-109) ist mit einem farbcodierten fluoreszierenden Körper (108) und einer dem fluoreszierenden Körper gegenüberliegend angeordneten Elektronenquelle (101-104) mit einer Elektronen emittierenden Einrichtung (102) für jedes der Pixel.

Revendications

1. Procédé d'attaque d'un panneau (20, 6) d'affichage en couleurs ayant des pixels (10) agencés en m rangées (L1-Lm) et n colonnes (D1-Dn) dans une formation en delta, codée, en couleurs RGB, pour afficher une image représentée par un signal d'image déterminé pour k lignes de balayage de trame effectives (o1-ok, e1-ek) pour chaque trame d'image impaire et paire (o, e) lequel procédé comprend des étapes de fonctionnement en mode normal consistant à exécuter une attaque avec interpolation de deux rangées de manière que l'écriture de données de ligne d'image obtenues à partir dudit signal d'image soit validée séquentiellement par ligne, et que des données de ligne d'image d'échantillonnage en phase et en opposition de phase (A, B), pour une ligne de balayage d'image correspondante, soient écrites sur certaines, respectives, de deux rangées consécutives de matrice (L1 & L2, L3 & L4, ...) pendant chaque période de balayage horizontal (1H, 2H, ...) dans un ordre alterné (A, B, A, B) les polarités de données de ligne (A, B) écrites à chaque rangée de la matrice alternant d'une rangée de matrice (L1, L3, ...) à la rangée de matrice suivante (L2, L4, ...) ou d'une paire de rangées de matrice (L1 & L2, L5 & L6, ...) à la paire suivante de rangées de matrice (L3 & L4, L7 & L6, ...)

caractérisé en ce que :

pour afficher une image pour laquelle le nombre k de lignes de balayage est différent de m et différent de m/2, et a une valeur comprise entre elles, ledit procédé est modifié par des étapes de fonctionnement en mode de compression qui sont toutes exécutées de façon répétée après des nombres respectifs de périodes de balayage horizontal (2H, 6H, ...3H, 7H...), lesdites étapes de fonctionnement en mode de compression consistant :

à interrompre ladite attaque avec interpolation de deux rangées à la suite de l'écriture de la première desdites données de ligne d'image d'échantillonnage en phase ou en opposition de phase (A, B) sur la première des deux rangées consécutives de matrice écrites dans la période de balayage horizontal suivante (3H, 7H, ..., 4H, 7H) ;

à supprimer l'écriture de la seconde desdites données de ligne d'image d'échantillonnage en phase ou en opposition de phase (A, B) qui devrait être écrite à la seconde desdites deux rangées consécutives de la matrice ; et

à reprendre ladite attaque avec interpolation de deux rangées pour la période de balayage horizontal immédiatement suivante (4H, 8H, ...5H, 9H) en commençant avec l'écriture sur ladite seconde desdites deux rangées consécutives, où l'ordre d'alternance (A, B, A, B) d'écriture desdites données de ligne d'image d'échantillonnage en phase et en opposition de phase est inversé (B, A, B, A, ...) et la séquence d'alternance de polarité des signaux d'image écrits est maintenue sans interruption.

2. Procédé selon la revendication 1 dans lequel lesdites données de ligne d'image d'échantillonnage en phase et en opposition de phase sont écrites avec une première polarité et la polarité opposée dans chaque trame impaire et avec l'inverse de ladite polarité et de la polarité opposée dans chaque trame paire.

3. Procédé selon la revendication 1, dans lequel, pendant ladite attaque avec interpolation de deux ran-

gées, lesdites données de ligne d'image d'échantillonnage en phase et en opposition de phase sont écrites avec des polarités qui sont inversées pour chaque période de balayage horizontal alternée, lesquelles données de ligne d'image d'échantillonnage en phase et en opposition de phase écrites dans des périodes de balayage horizontal respectives ont la même polarité respective (A^+ & B^+, A^- & B^-) lorsqu'elles sont écrites dans ledit ordre alterné (A, B, A, B) et ont une polarité respective opposée (A^- & B^+, A^+ & B^-) lorsqu'elles sont écrites dans l'ordre alterné inversé (B, A, B, A, ...).

4. Procédé selon l'une quelconque des revendications 1 à 3 appliqué à un panneau d'affichage en couleurs à cristaux liquides à matrice active (6 : figure 14).

5. Procédé selon l'une quelconque des revendications 1 à 3 appliqué à un panneau (101- 109) d'affichage en couleurs à émission d'électrons comportant un corps fluorescent (108) codé en couleurs et une source d'électrons (101-104), ayant un dispositif d'émission d'électrons (102) pour chacun desdits pixels, agencée de façon à être opposée audit corps fluorescent.

6. Appareil d'affichage en couleurs pouvant fonctionner conformément au procédé de la revendication 1, comportant :

un panneau (6, 20) d'affichage en couleurs ayant des pixels (10) agencés en m rangées (L1-Lm) et n colonnes (D1-Dn) dans une formation en delta codée en couleurs RGB, pour afficher une image représentée par un signal d'image ayant k lignes de balayage de trame effectives (o1-ok, e1-ek) pour chacune des trames d'image impaires et paires ;
des moyens d'attaque destinés à attaquer ledit panneau d'affichage d'une manière en interpolation de deux rangées, lesdits moyens d'attaque comprenant :

des moyens d'écriture (80-1, 80-2, 100-1, 100-2, 120-1, 120-2) destinés à écrire des données de ligne d'image d'échantillonnage en phase et en opposition de phase (A, B), formant des paires, chaque paire correspondant à des lignes de balayage respectives de l'image représentée par le signal d'image, sur des paires respectives de première et seconde rangées consécutives d'une matrice, les polarités des données de ligne (A, B) devant être écrites sur chaque rangée de matrice alternant d'une rangée de matrice (L1, L3, ...) à la rangée de matrice suivante (L2, L4, ...) ou d'une paire de rangées de matrice consécutives (L1 & L2, L5 & L6, ...) à la paire suivante de rangées de matrice consécutives (L3 & L4, L7 & L8, ...) ;
des moyens de sélection (40, 60, ..1-1 à 1-3, 2-1 à 2-3) destinés à sélectionner séquentiellement ladite ligne de rangées de matrice pour écrire lesdites données de ligne, deux rangées consécutives de matrice à deux temps consécutifs dans chaque période de balayage horizontal ; et
des moyens de commande (140) agencés de façon à commander lesdits moyens d'écriture et lesdits moyens de sélection, pour commander les temps relatifs et la séquence de leur fonctionnement ;

caractérisé en ce que :

pour afficher une image pour laquelle le nombre k de lignes de balayage est différent de n et différent de m/2 et a une valeur comprise entre eux, lesdits moyens d'attaque sont conçus pour effectuer lesdites étapes de fonctionnement dans le mode de compression et comprennent donc :

des moyens destinés à interrompre l'attaque avec interpolation de deux rangées ;
des moyens destinés à supprimer ladite écriture de la seconde des données de ligne d'image d'échantillonnage en phase et en opposition de phase ; et
des moyens destinés à reprendre ladite attaque avec interpolation de deux rangées.

7. Appareil selon la revendication 6, dans lequel, lesdits moyens de sélection (40, 60, ..., 1-1 à 1-3, 2-1 à 2-3) comprennent :

un premier groupement de commutateurs (1-1 à 1-3, ...) connecté entre des rangées de matrice impaires (L1, L3, L5, ...) du panneau d'affichage et une première ligne de commande pour appliquer en entrée un premier signal de tension de balayage (ΦG_o) ;
un deuxième groupement de comutateurs (2-1 à 2-3, ...) connecté entre des rangées de matrice paires (L2, L4, L6, ...) du panneau d'affichage et une seconde ligne de commande pour appliquer en entrée un deuxième signal de tension de balayage (ΦG_o) ;
un troisième groupement de commutateurs (3-1 à 3-3, ...) connecté entre la troisième et les rangées de matrice impaires suivantes (L3, L5, L7, ...) du panneau d'affichage et une troisième ligne de commande pour appliquer en entrée un troisième signal de tension de balayage (ΦG) ; et

des moyens (40) de génération de signaux de déclenchement destinés à générer des signaux de déclenchement séquentiels respectifs (V1, V2, V3, ...) et à appliquer chacun d'eux à un groupe respectif de trois commutateurs, un commutateur (1-1, 2-1 & 3-1 ; 1-2, 2-2, 3-2, ...) dans chacun des premier, deuxième et troisième groupements ;
lesdits moyens de commande fournissent lesdits premier à troisième signaux de tension de balayage (ΦG_o, ΦG_e, ΦG), lesquels signaux (ΦG_o, ΦG_e) déclenchés par lesdits commutateurs desdits premier et deuxième groupements sont destinés à valider une attaque avec interpolation de deux rangées dans ledit ordre alterné,
lesquels signaux (ΦG_e, ΦG) déclenchés par lesdits commutateurs desdits deuxième et troisième groupements sont destinés à valider une attaque avec interpolation de deux rangées dans ledit ordre alterné inverse, et
lesquels signaux (ΦG_e, ΦG) déclenchés respectivement par lesdits commutateurs desdits deuxième et troisième groupements sont destinés à supprimer une écriture à la suite d'une interruption de ladite attaque avec interpolation de deux rangées dans ledit ordre alterné et dans ledit ordre alterné inverse, respectivement ; et
lesdits moyens de commande sont agencés de façon à commander lesdits moyens de génération de signaux de déclenchement pour générer et fournir des signaux de déclenchement modifiés (V3, ...) afin de faciliter l'écriture, à partir de la seconde de deux rangées consécutives, à chaque fois qu'une attaque avec interpolation de deux rangées est reprise.

8. Appareil selon la revendication 7, dans lequel lesdits moyens d'écriture comprennent des mémoires de lignes respectives (100-1, 100-2) destinées à stocker les données de ligne d'image d'échantillonnage en phase et en opposition de phase qui doivent être utilisées lors d'une écriture sur le panneau d'affichage.

9. Appareil selon l'une quelconque des revendications 6 à 8, dans lequel ledit panneau (20) d'affichage en couleurs est un panneau d'affichage à cristaux liquides à matrice active (6 : figure 14).

10. Appareil selon l'une quelconque des revendications 6 à 8, dans lequel ledit panneau (20) d'affichage en couleurs est un panneau (101-109) d'affichage en couleurs à émission d'électrons comportant un corps fluorescent (108) codé en couleurs et une source d'électrons (101-104) ayant un dispositif d'émission d'électrons (102) pour chacun desdits pixels, agencée de façon à être opposée audit corps fluorescent.

FIG. 1

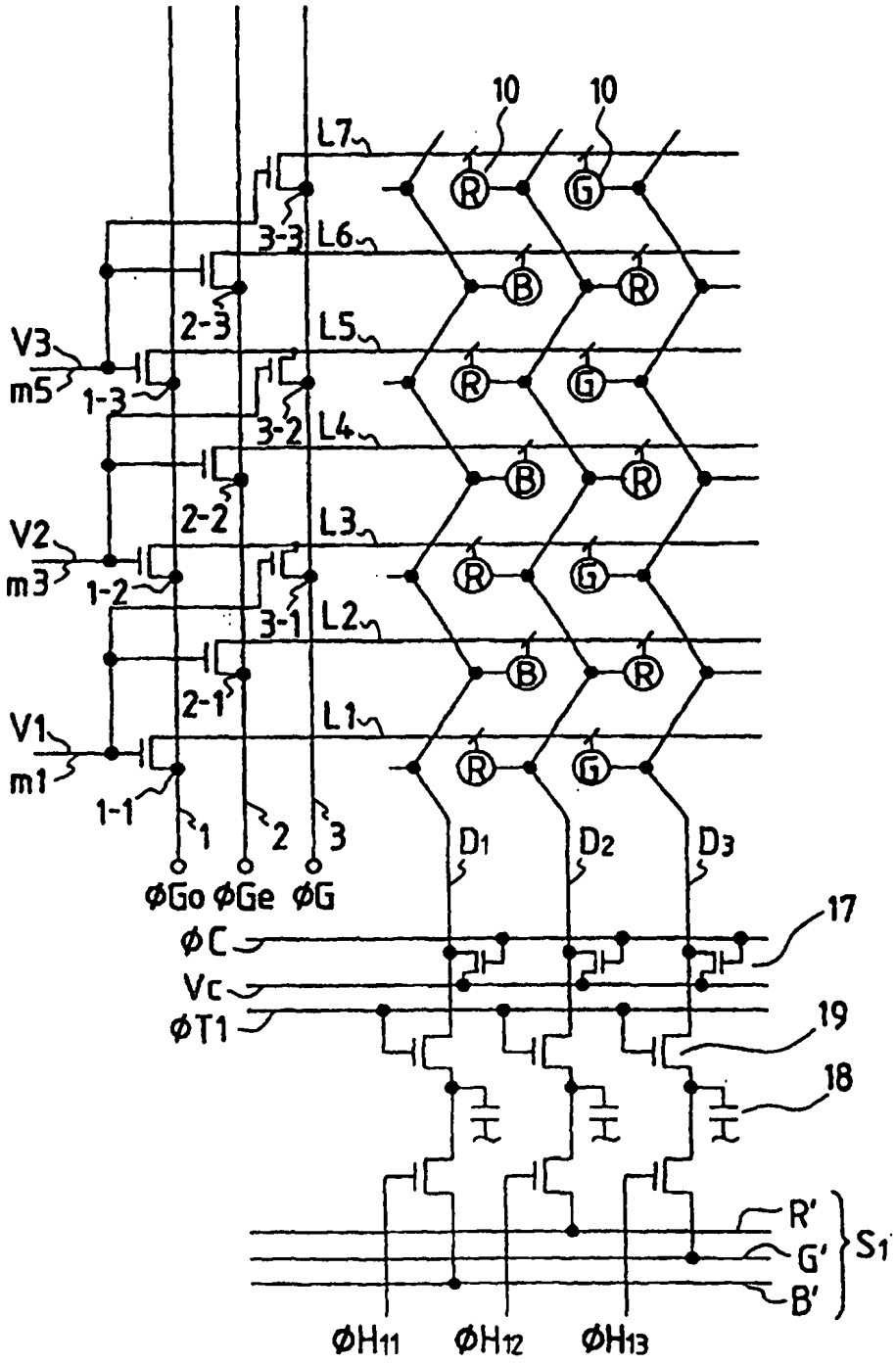

10
10
L7
3-3
L6
2-3
L5
V3
m5
1-3
3-2
L4
2-2
L3
V2
m3
1-2
3-1
L2
2-1
L1
V1
m1
1-1
1
2
3
D1
D2
D3
ΦGo ΦGe ΦG
ΦC
17
Vc
ΦT1
19
18
R'
G'
B'
S1
ΦH11
ΦH12
ΦH13

FIG. 2

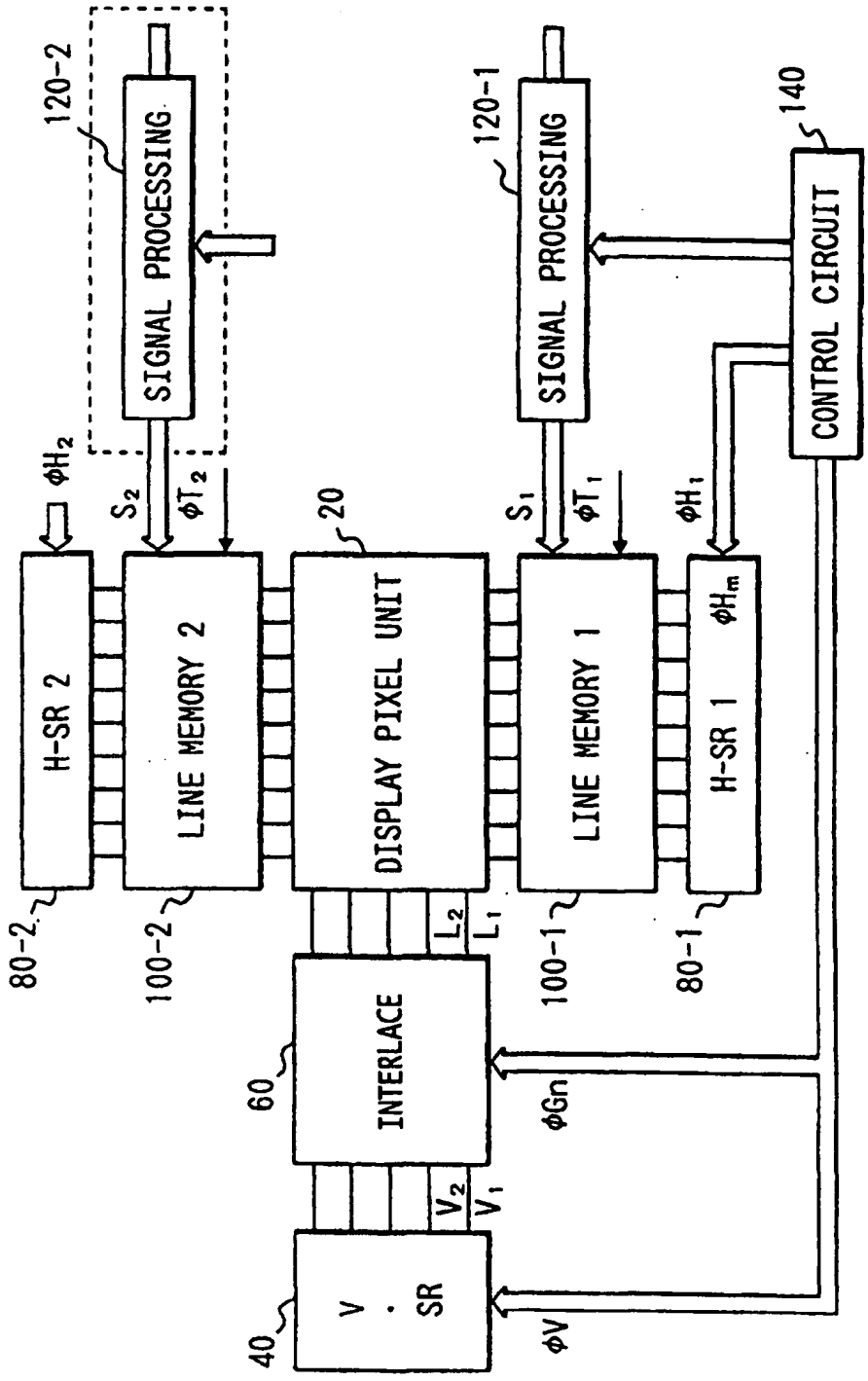

120-2
SIGNAL PROCESSING
120-1
SIGNAL PROCESSING
140
CONTROL CIRCUIT
φH2
S2
φT2
20
S1
φT1
φH1
H-SR 2
LINE MEMORY 2
DISPLAY PIXEL UNIT
LINE MEMORY 1
H-SR 1
φHm
80-2
100-2
L2
L1
100-1
80-1
60
INTERLACE
φGn
V2
V1
40
V · SR
φV

FIG. 3

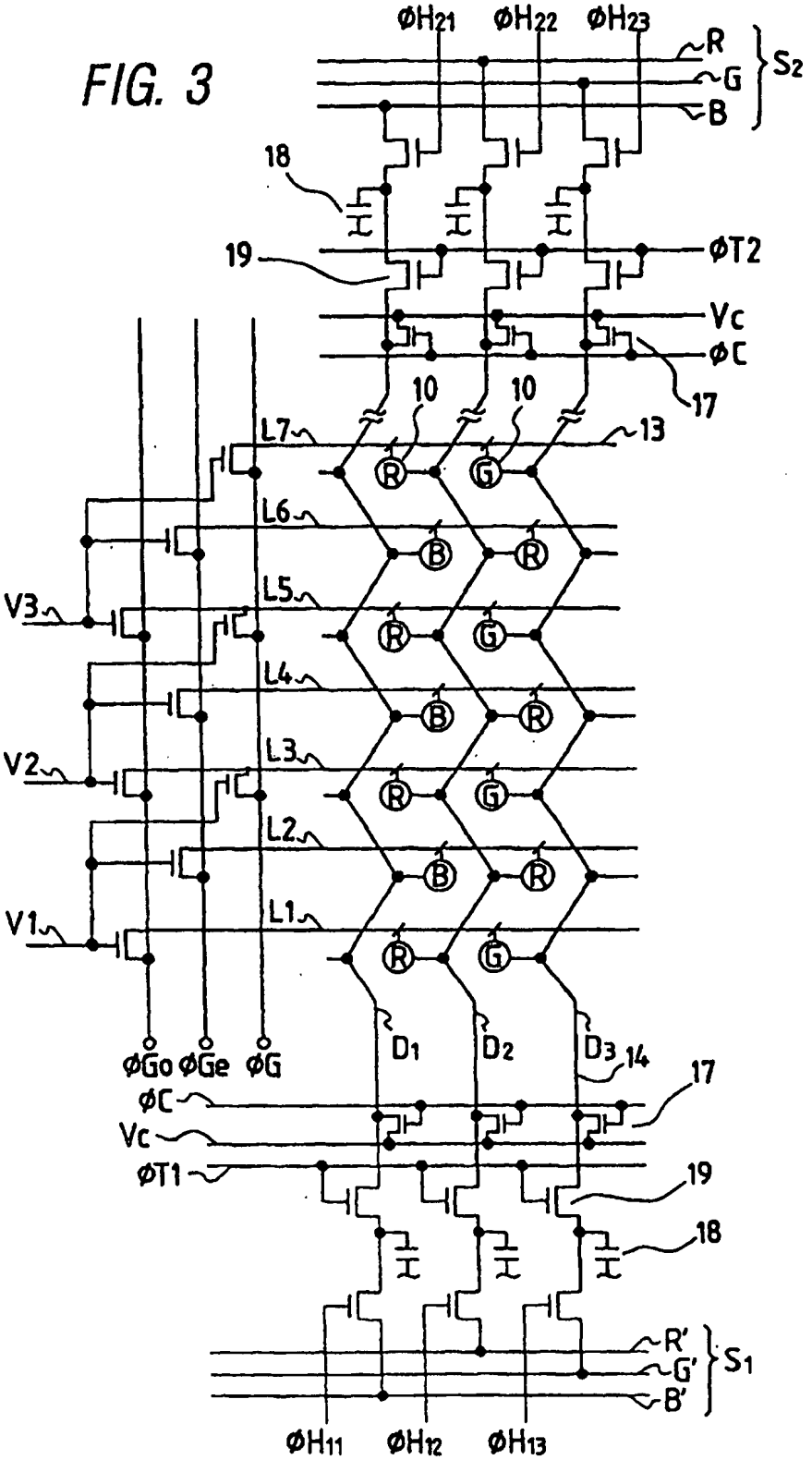

ØH21
ØH22
ØH23
R
G
B
S2
18
19
ØT2
Vc
ØC
17
10
10
L7
13
L6
L5
V3
L4
L3
V2
L2
L1
V1
ØGo
ØGe
ØG
D1
D2
D3
14
17
ØC
Vc
ØT1
19
18
R'
G'
B'
S1
ØH11
ØH12
ØH13

FIG. 4

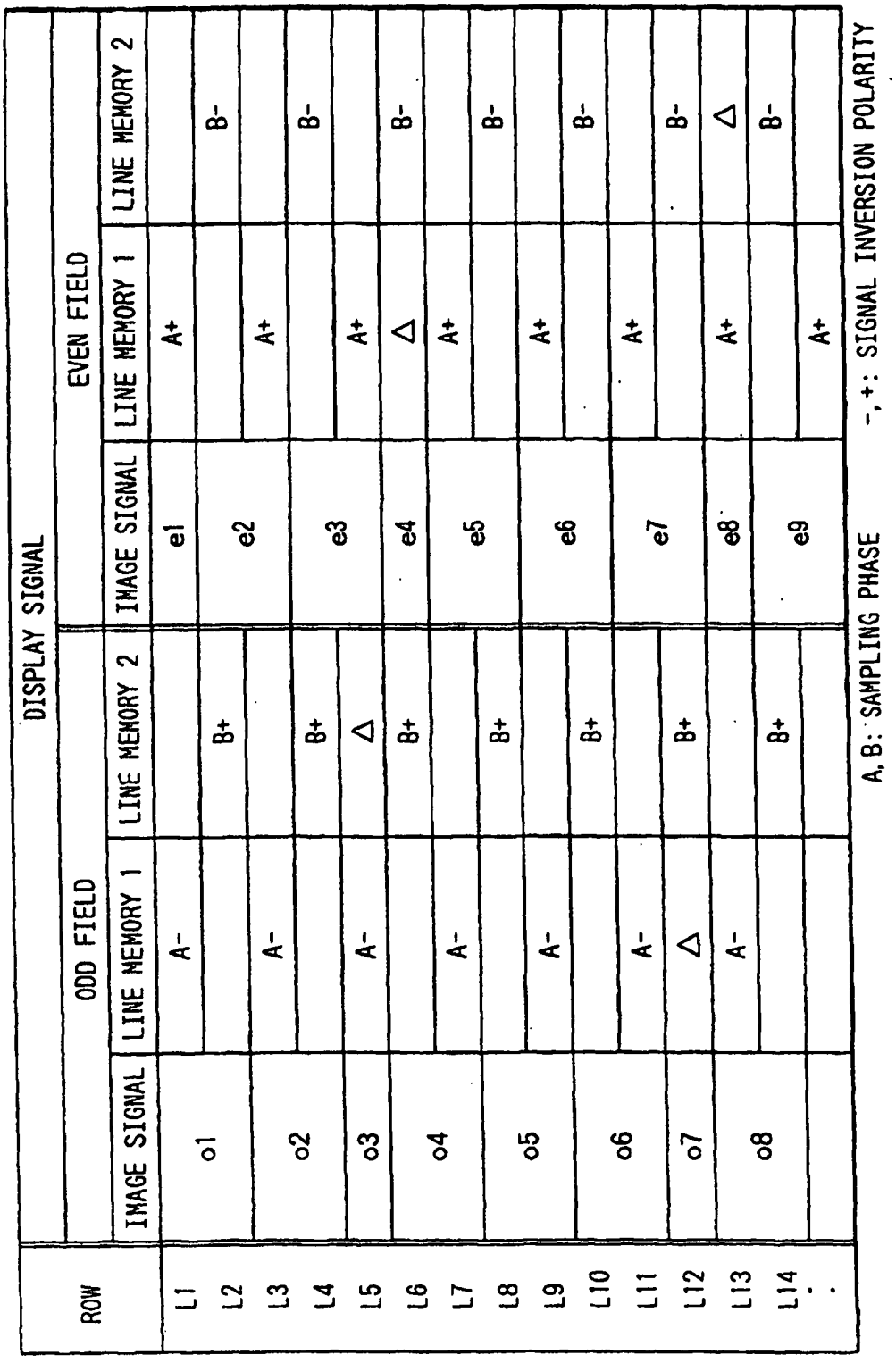

DISPLAY SIGNAL
ROW
ODD FIELD
EVEN FIELD
IMAGE SIGNAL
LINE MEMORY 1
LINE MEMORY 2
IMAGE SIGNAL
LINE MEMORY 1
LINE MEMORY 2
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
o1
o2
o3
o4
o5
o6
o7
o8
e1
e2
e3
e4
e5
e6
e7
e8
e9
A-
B+
A+
B-
A, B: SAMPLING PHASE
-,+: SIGNAL INVERSION POLARITY

FIG. 5A

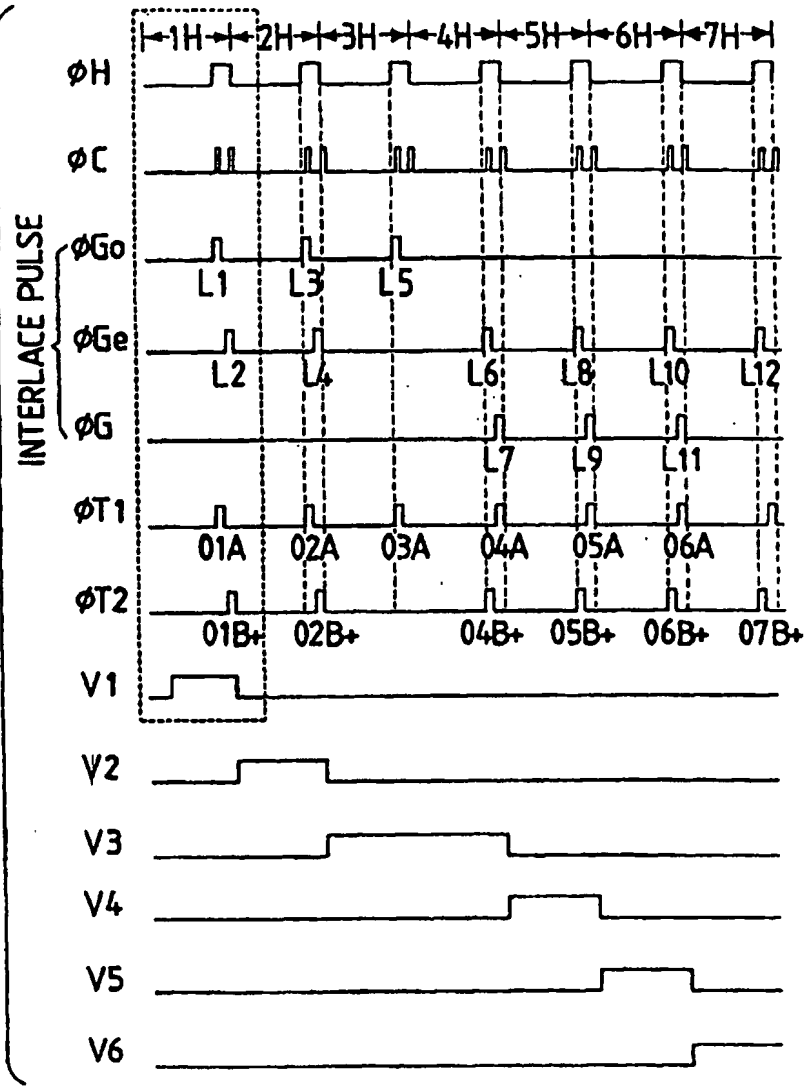

1H
2H
3H
4H
5H
6H
7H
INTERLACE PULSE
φH
φC
φGo
φGe
φG
φT1
φT2
V1
V2
V3
V4
V5
V6
L1
L3
L5
L2
L4
L6
L8
L10
L12
L7
L9
L11
01A
02A
03A
04A
05A
06A
01B+
02B+
04B+
05B+
06B+
07B+

FIG. 5B

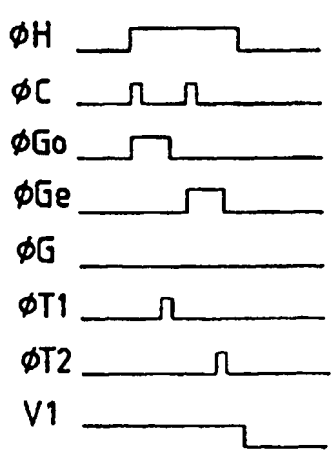

φH
φC
φGo
φGe
φG
φT1
φT2
V1

FIG. 6

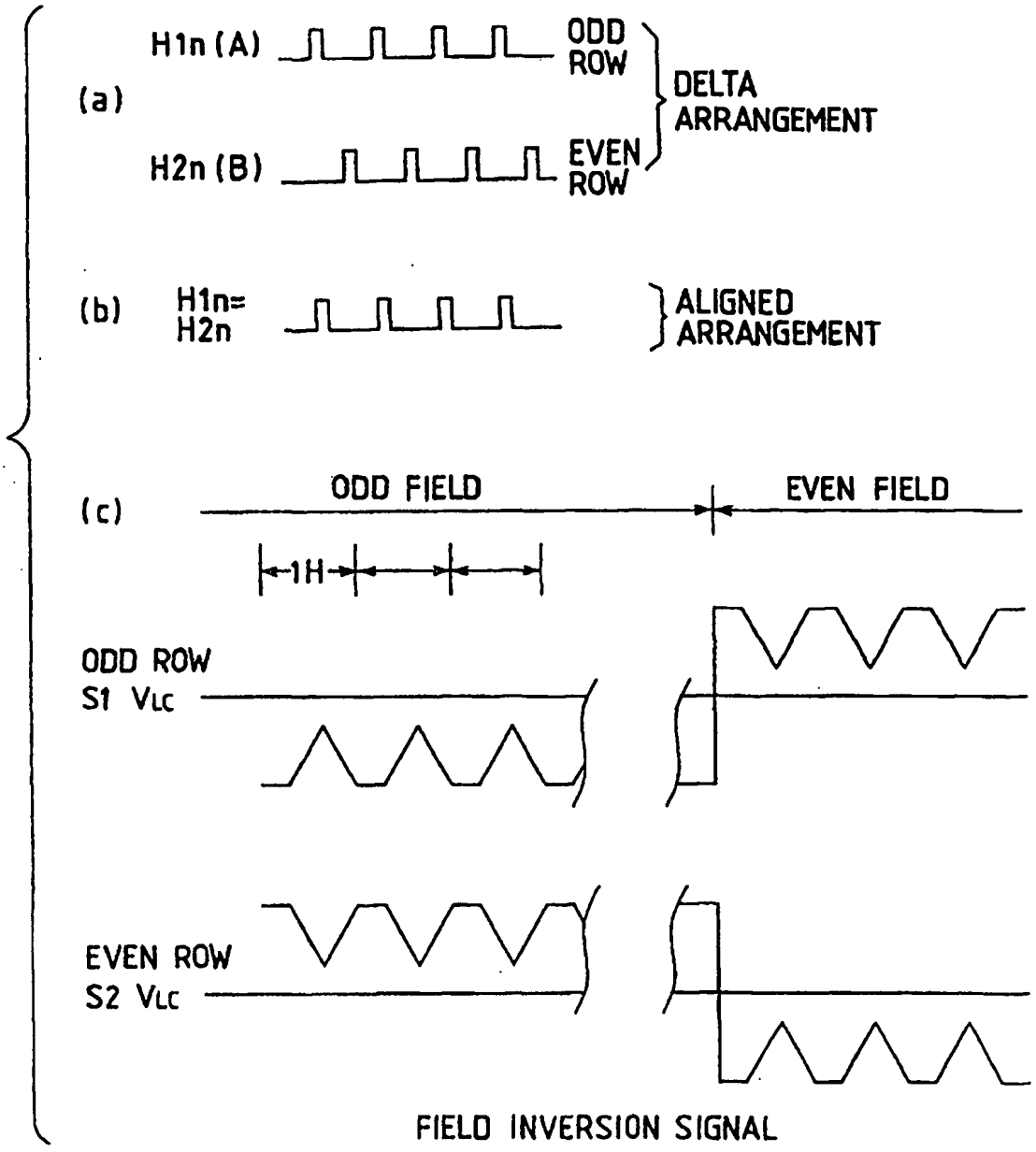

(a)
H1n (A)
ODD ROW
H2n (B)
EVEN ROW
DELTA ARRANGEMENT
(b)
H1n= H2n
ALIGNED ARRANGEMENT
(c)
ODD FIELD
EVEN FIELD
1H
ODD ROW
S1 VLC
EVEN ROW
S2 VLC
FIELD INVERSION SIGNAL

FIG. 7A

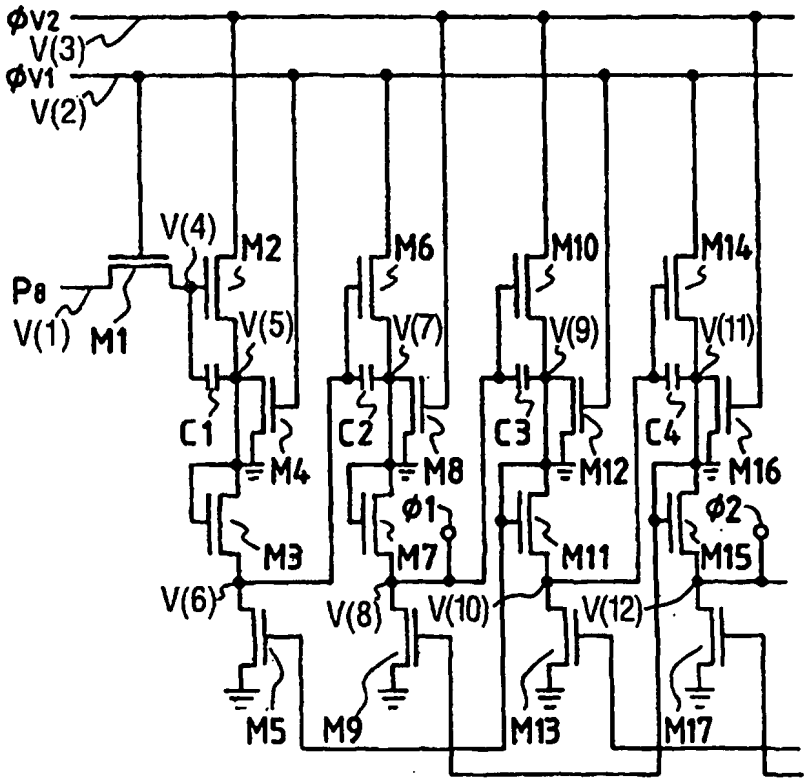
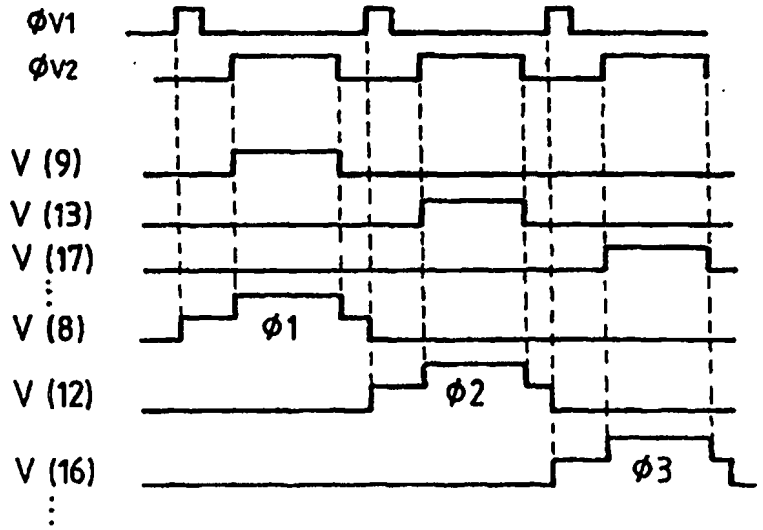

φV2
V(3)
φV1
V(2)
V(4)
M2
M6
M10
M14
PB
V(1)
M1
V(5)
V(7)
V(9)
V(11)
C1
C2
C3
C4
M4
M8
M12
M16
φ1
φ2
M3
M7
M11
M15
V(6)
V(8)
V(10)
V(12)
M5
M9
M13
M17

FIG. 7B


φV1
φV2
V (9)
V (13)
V (17)
V (8)
φ1
V (12)
φ2
V (16)
φ3

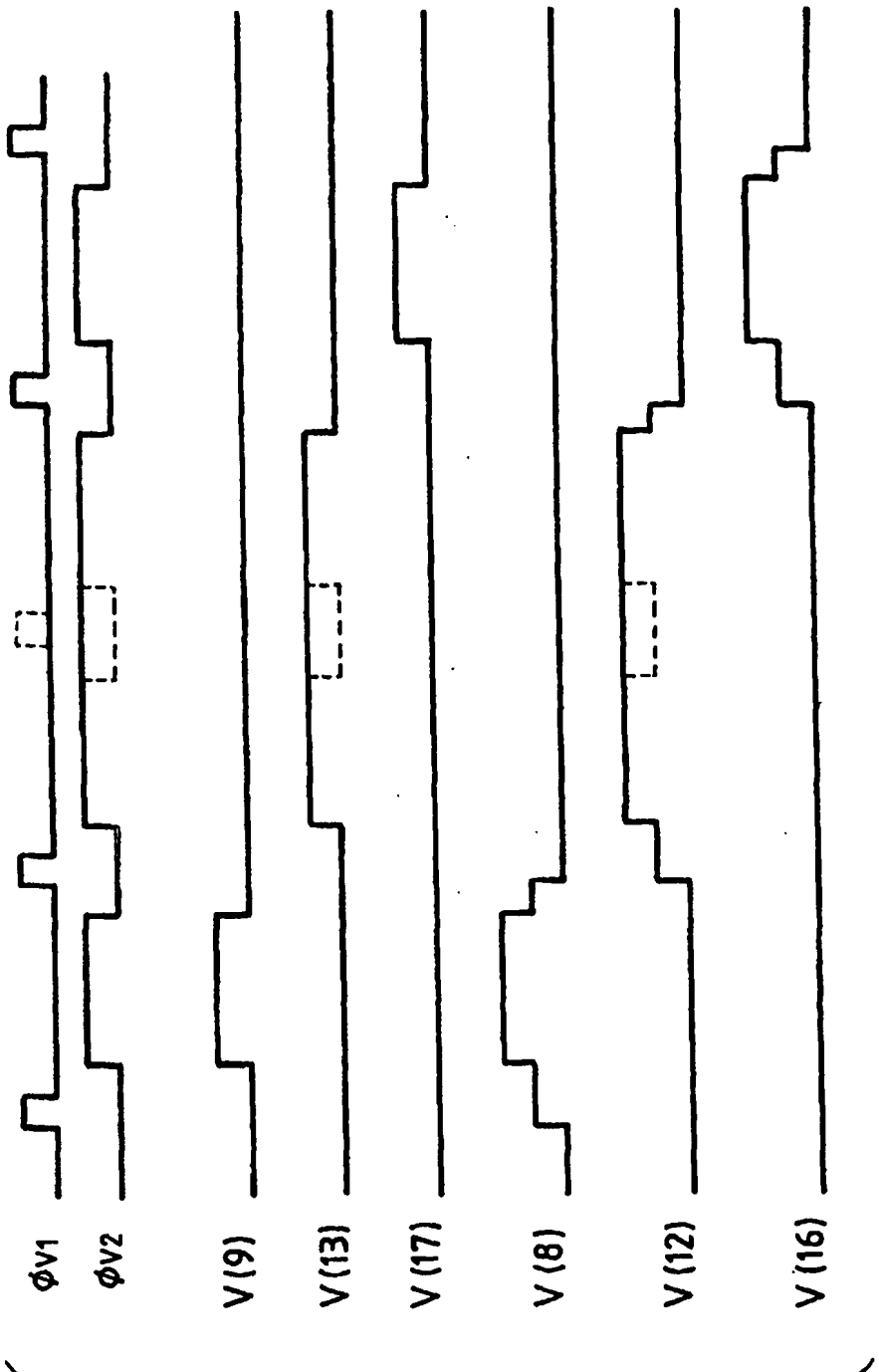


FIG. 8

FIG. 9

ROW	DISPLAY SIGNAL		
	ODD FIELD		
	IMAGE SIGNAL	LINE MEMORY 1	LINE MEMORY 2
L_1	01	A-	
L_2			B+
L_3	02		A-
L_4		B+	
L_5	03	A-	Δ
L_6	04	B+	
L_7			A-
L_8	05		B+
L_9		A-	
L_{10}	06	B+	
L_{11}			A-
L_{12}	07	Δ	B+
L_{13}	08		A-
L_{14}		B+	

FIG. 10

ROW	DISPLAY SIGNAL		
	ODD FIELD		
	IMAGE SIGNAL	LINE MEMORY 1	LINE MEMORY 2
L_1	01	A+	
L_2			B+
L_3	02	A-	
L_4			B-
L_5	03	A+	Δ
L_6	04		B+
L_7		A-	
L_8	05		B-
L_9		A+	
L_{10}	06		B+
L_{11}		A-	
L_{12}	07	Δ	B-
L_{13}	08	A+	
L_{14}			B+

FIG. 11

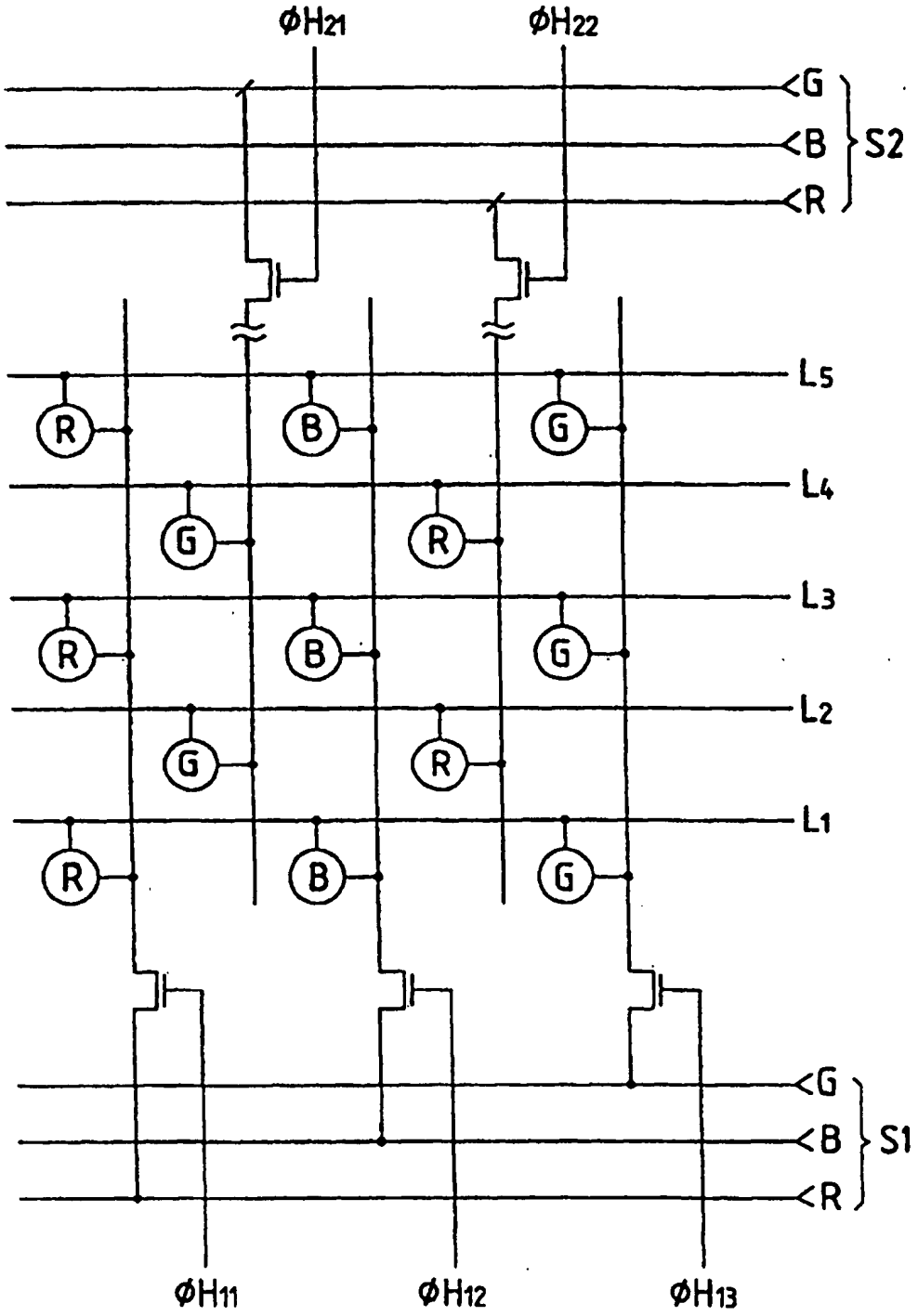

ΦH21
ΦH22
G
B
R
S2
L5
L4
L3
L2
L1
R
B
G
G
R
R
B
G
R
B
G
G
R
S1
ΦH11
ΦH12
ΦH13

FIG. 12

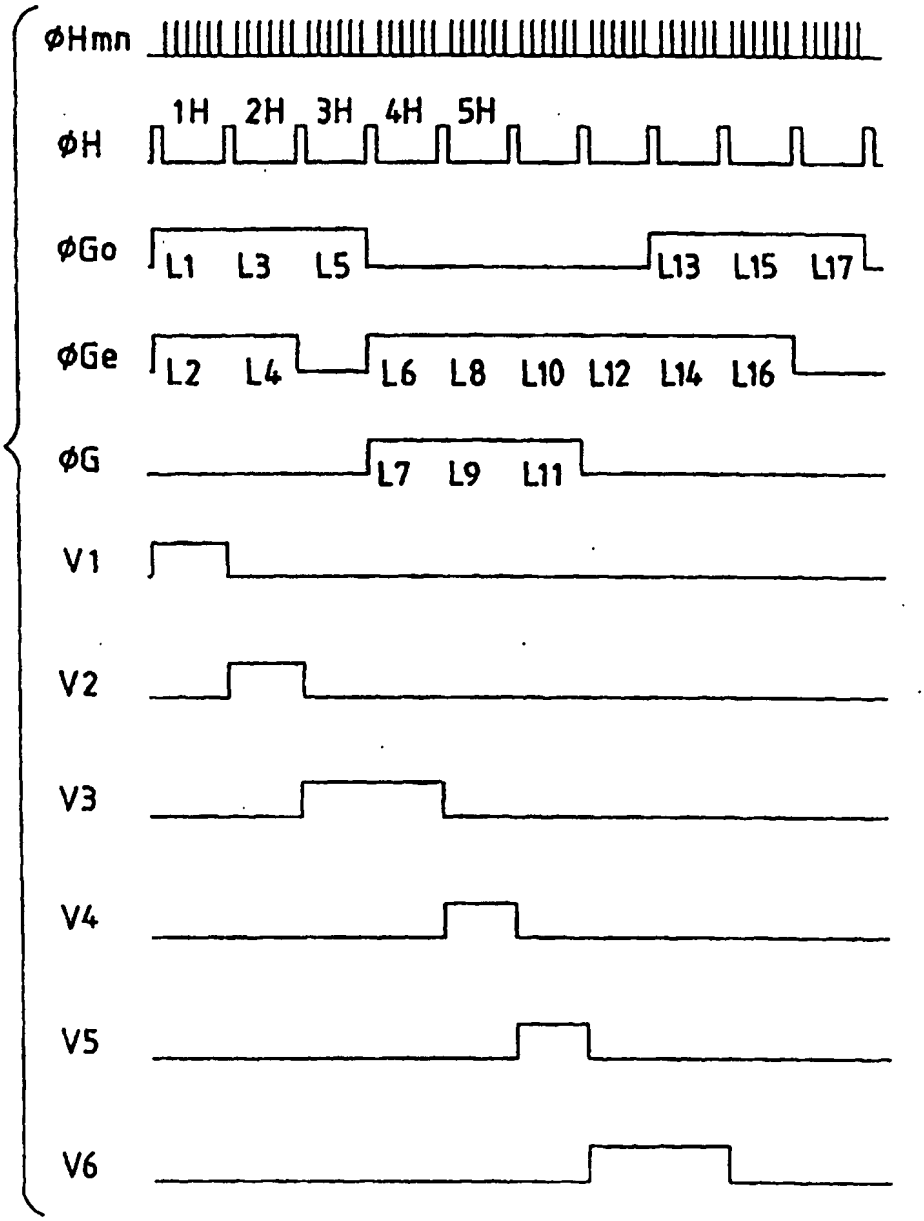

ØHmn
1H
2H
3H
4H
5H
ØH
ØGo
L1
L3
L5
L13
L15
L17
ØGe
L2
L4
L6
L8
L10
L12
L14
L16
ØG
L7
L9
L11
V1
V2
V3
V4
V5
V6

FIG. 13A

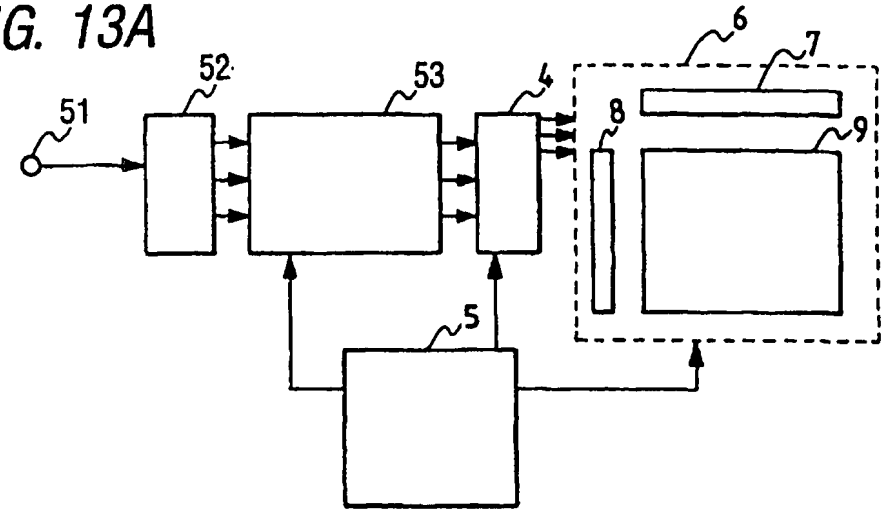


FIG. 13B

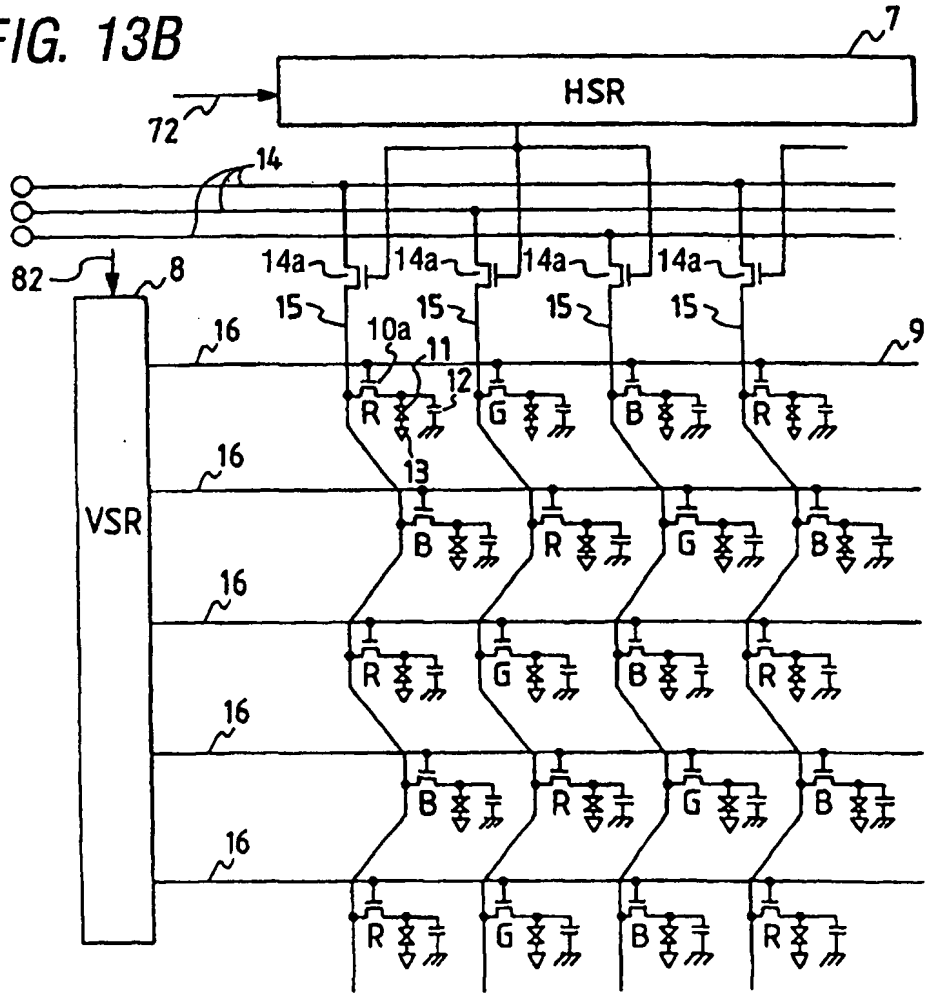


FIG. 14

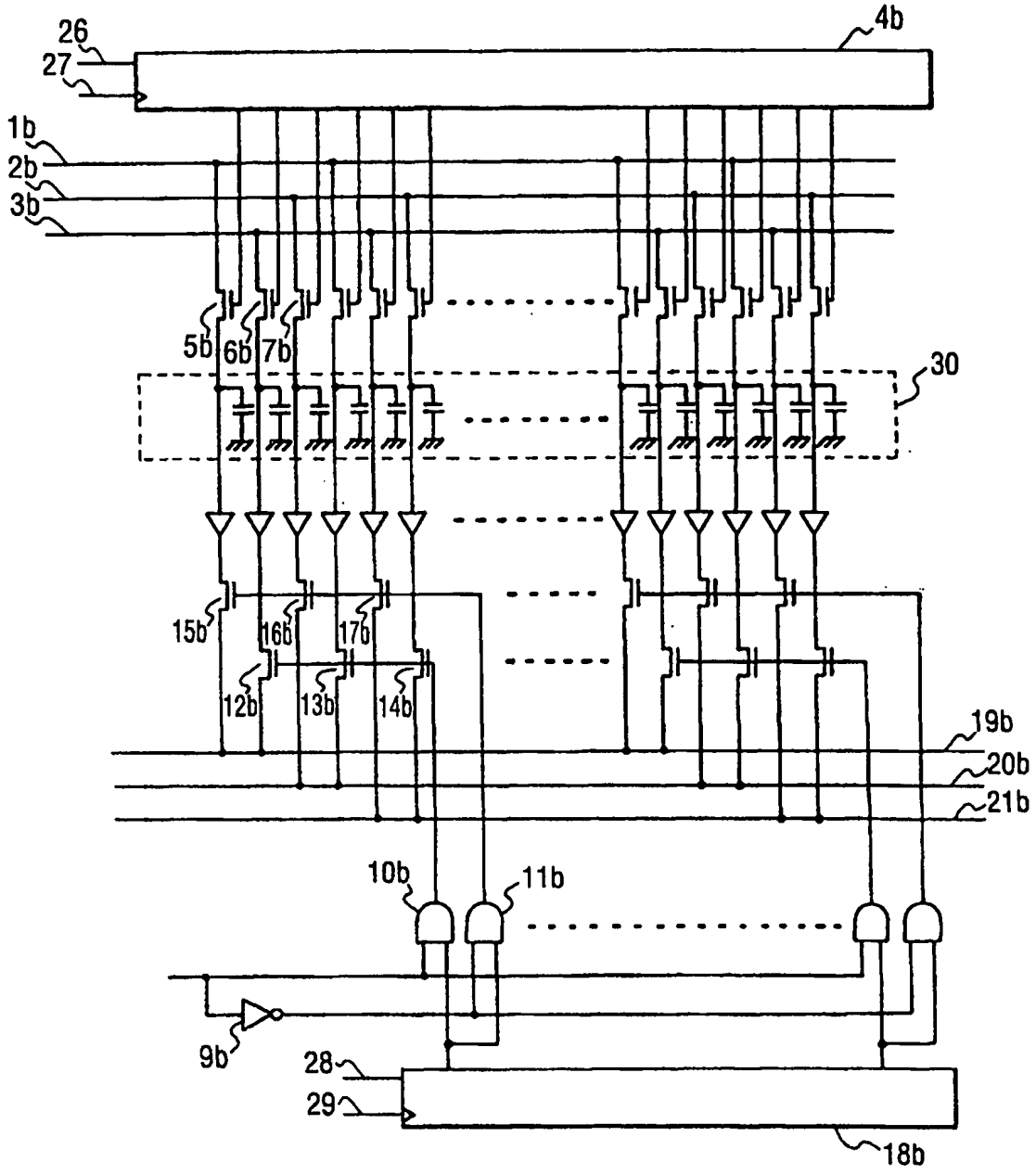

26
27
4b
1b
2b
3b
5b
6b
7b
30
15b
16b
17b
12b
13b
14b
19b
20b
21b
10b
11b
9b
28
29
18b

FIG. 15

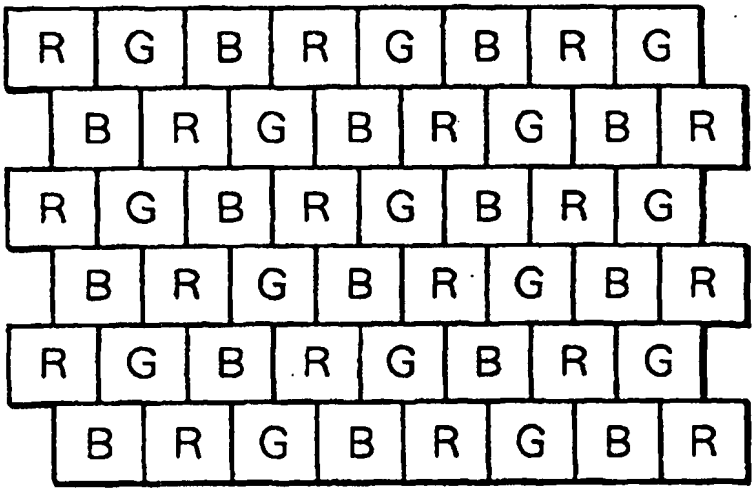


FIG. 17

	1st FIELD	2nd FIELD
⋮	⋮	⋮
2(k-1) ROW	O_{k-2}	E_{k-1}
2k-1 ROW	O'_{k-1}	E'_{k-1}
2k ROW	O_{k-1}	E_k
2(k+1)-1 ROW	O'_k	E'_k
2(k+1) ROW	O_k	E_{k+1}
⋮	⋮	⋮

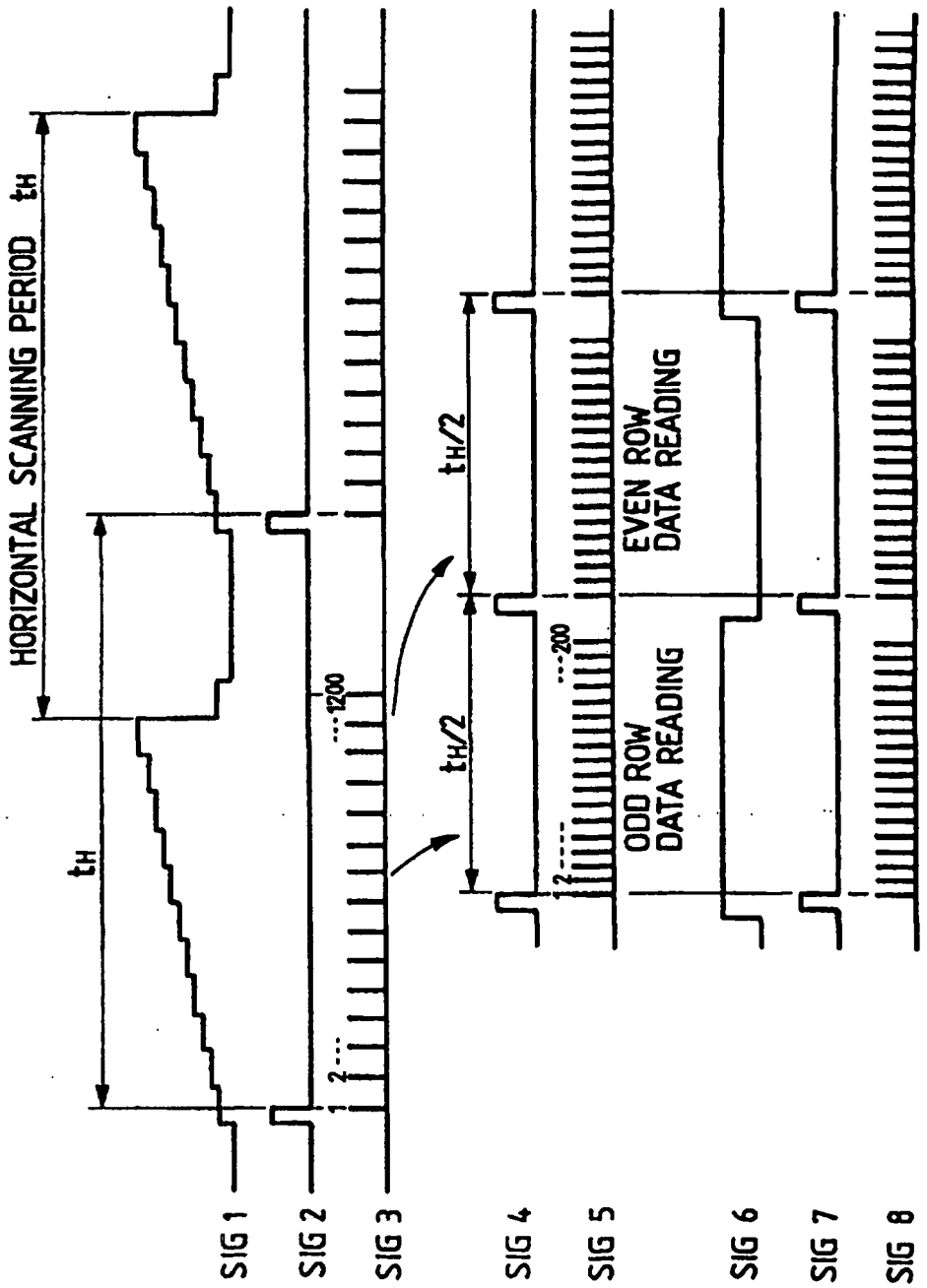

HORIZONTAL SCANNING PERIOD tH
tH
tH/2
tH/2
1
2
1200
200
ODD ROW DATA READING
EVEN ROW DATA READING
SIG 1
SIG 2
SIG 3
SIG 4
SIG 5
SIG 6
SIG 7
SIG 8

FIG. 16

FIG. 18

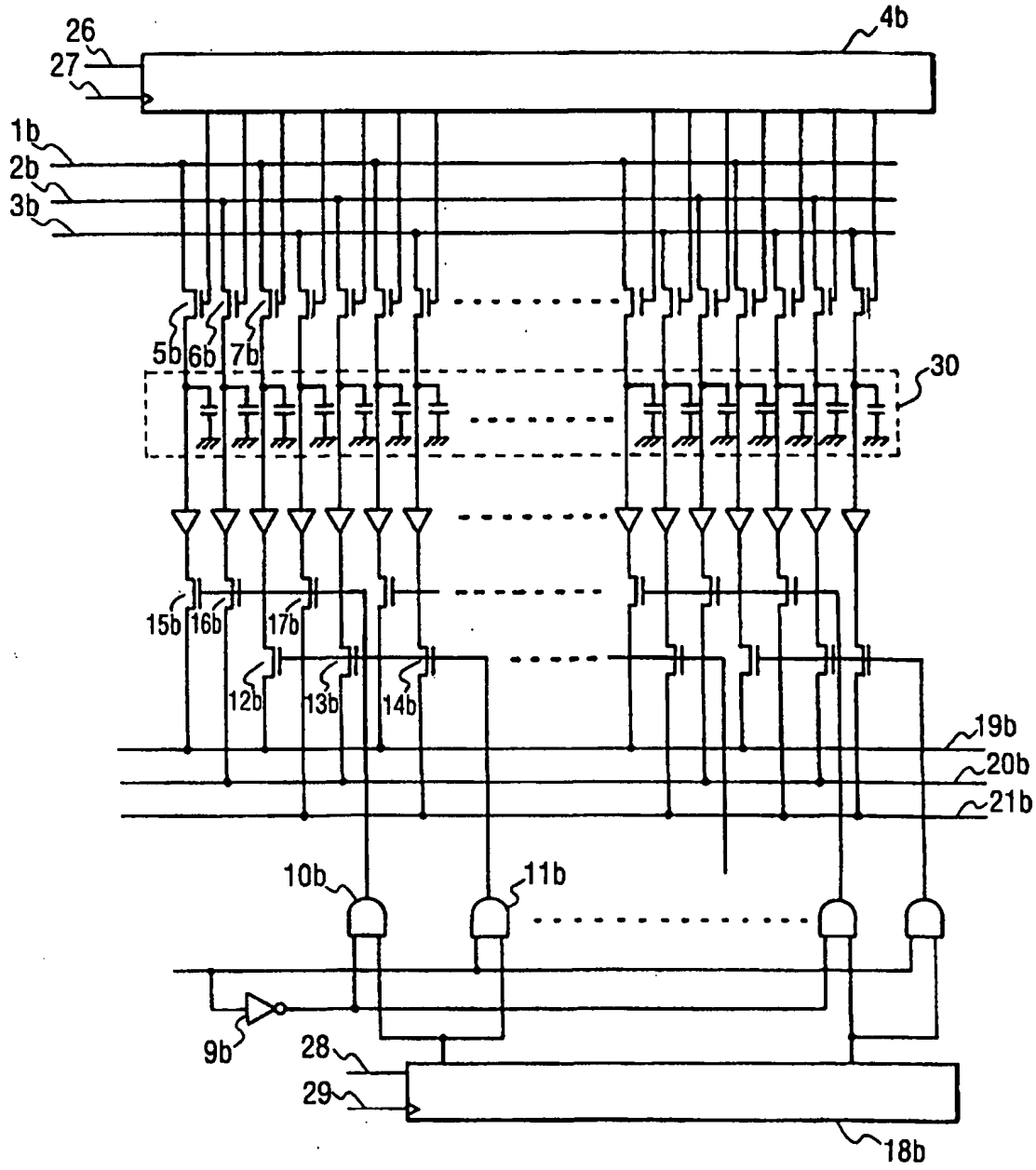

26
27
4b
1b
2b
3b
5b
6b
7b
30
15b
16b
17b
12b
13b
14b
19b
20b
21b
10b
11b
9b
28
29
18b

FIG. 19

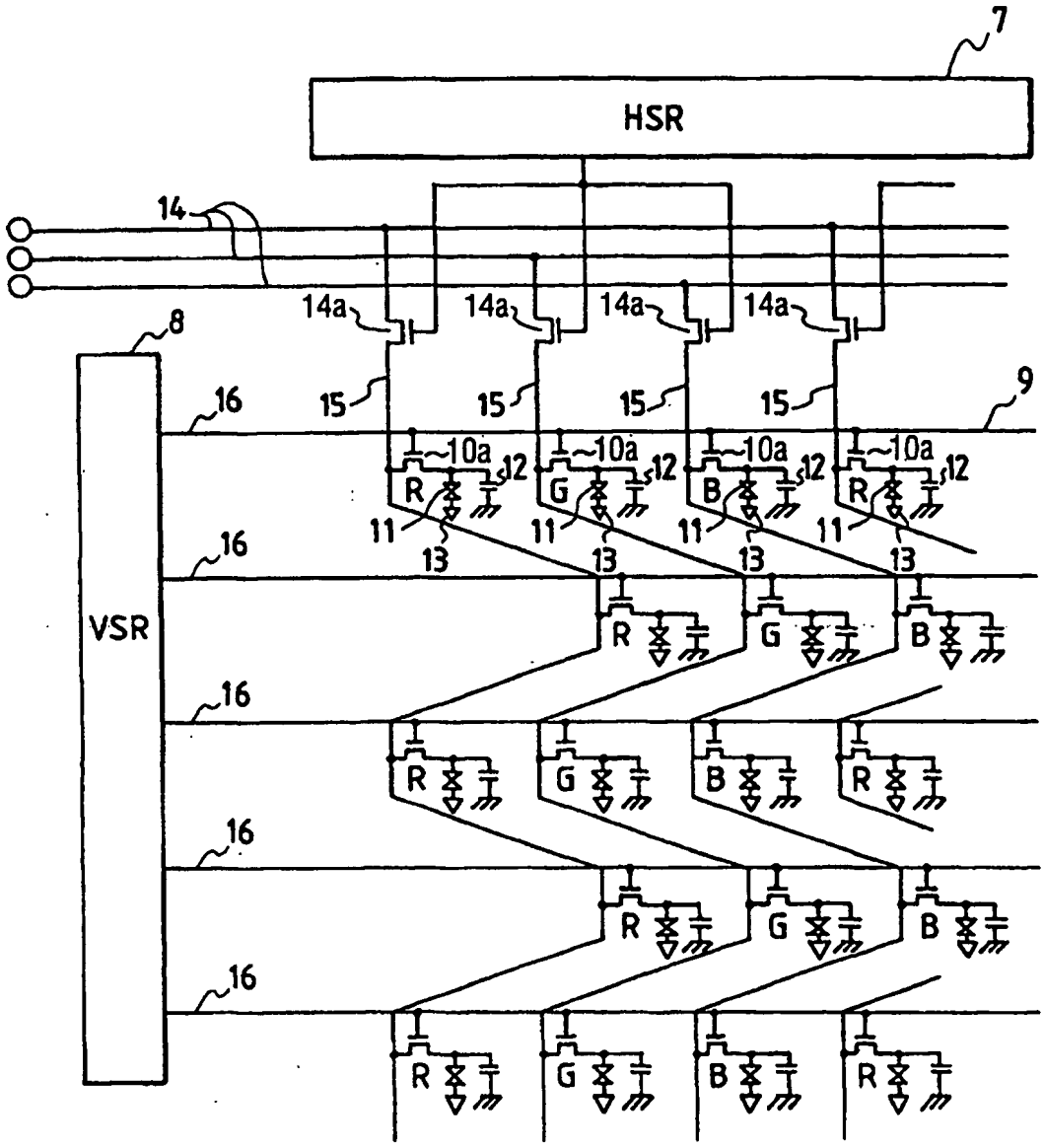
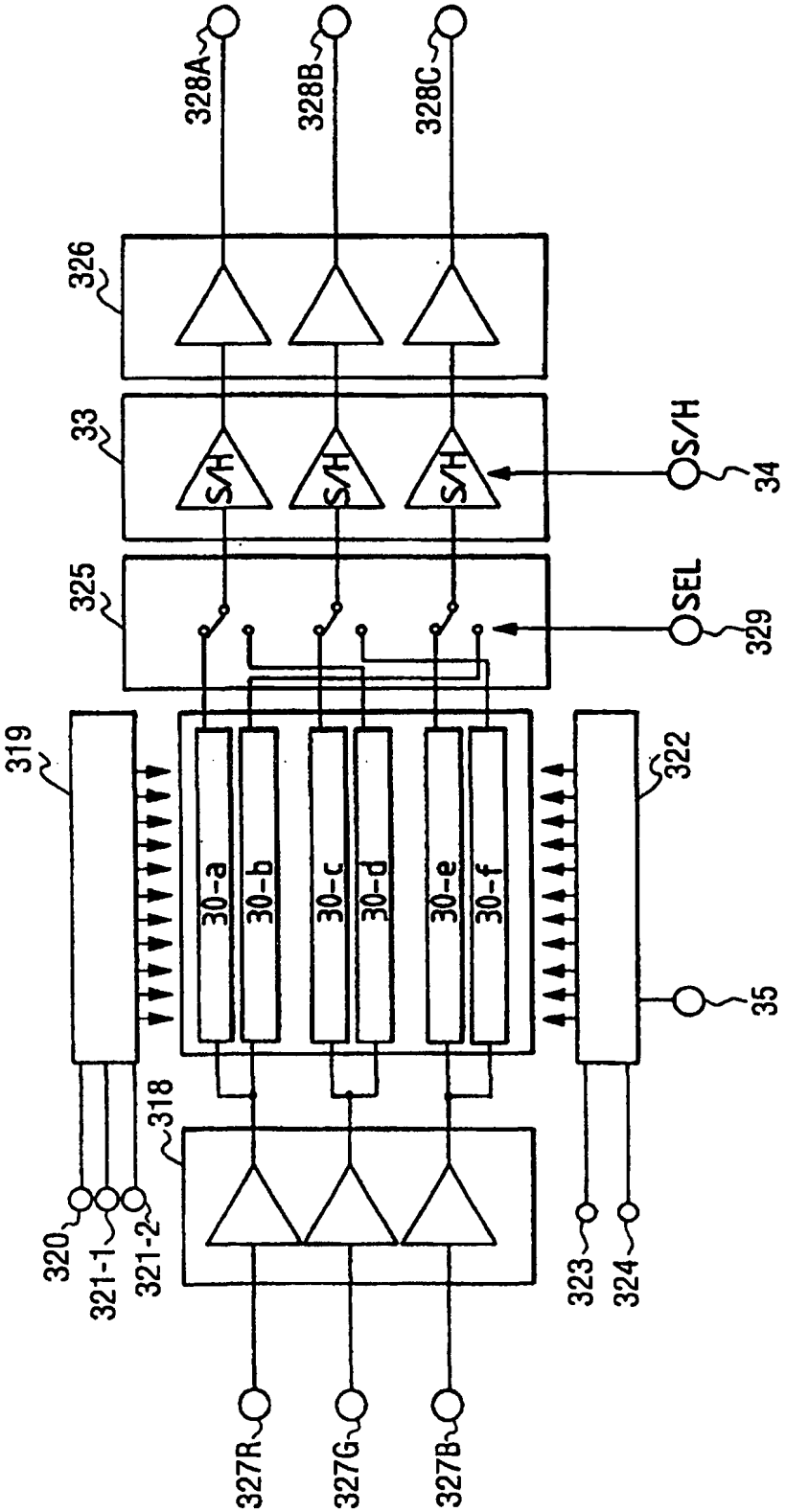


FIG. 20


328A
328B
328C
326
33
S/H
S/H
S/H
S/H
34
325
SEL
329
319
30-a
30-b
30-c
30-d
30-e
30-f
322
35
318
320
321-1
321-2
323
324
327R
327G
327B

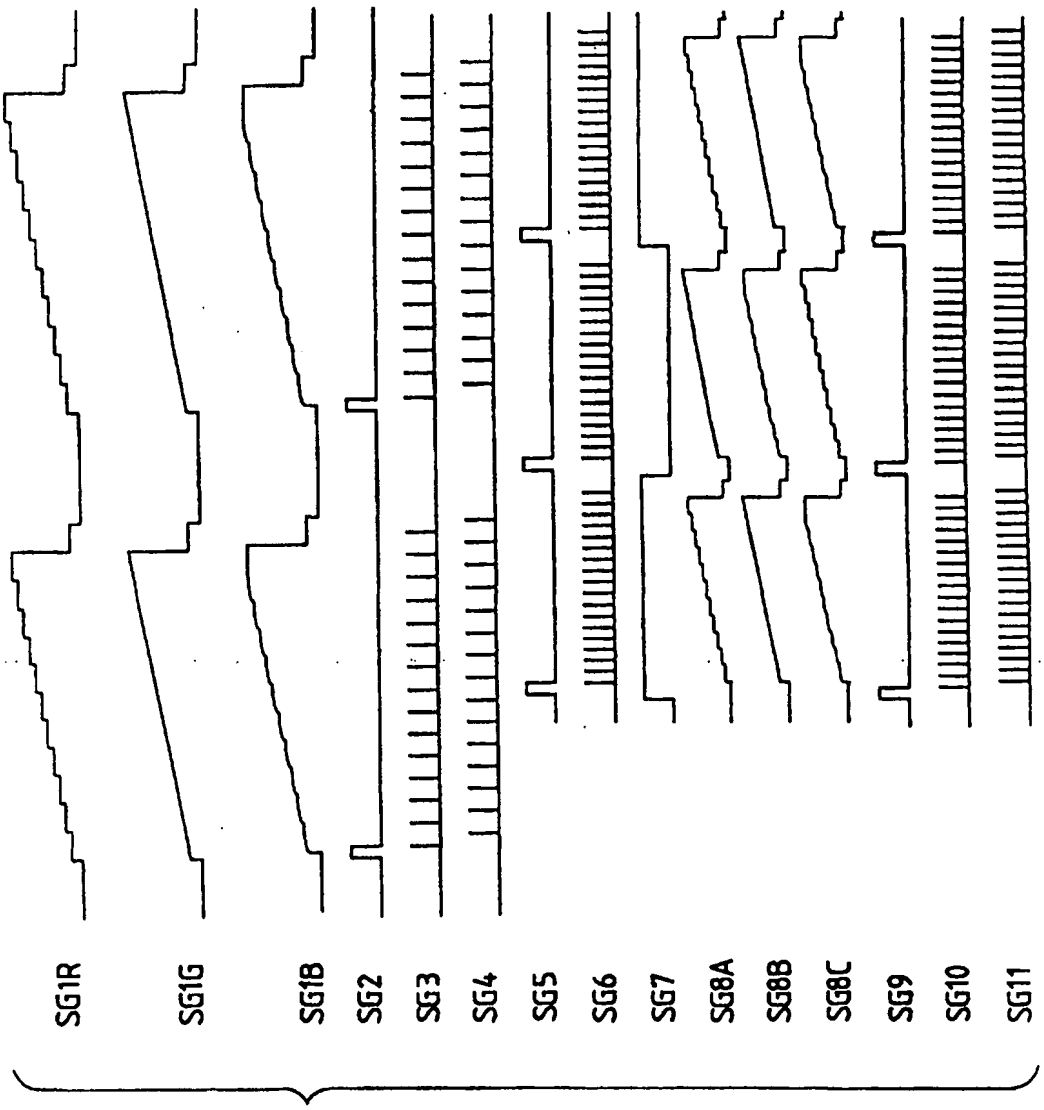

SG1R
SG1G
SG1B
SG2
SG3
SG4
SG5
SG6
SG7
SG8A
SG8B
SG8C
SG9
SG10
SG11

FIG. 21

FIG. 22

	1st FIELD	2nd FIELD	3rd FIELD	4th FIELD
2n ROW	O_{n-1} (1)	E_n (1)	O_{n-1} (2)	E_n (2)
2n+1 ROW	O_n· (1)	E_n· (1)	O_n· (2)	E_n· (2)
2(n+1) ROW	O_n (1)	E_{n+1} (1)	O_n (2)	E_{n+1} (2)
2n+3 ROW	O_{n+1}· (1)	E_{n+1}· (1)	O_{n+1}· (2)	E_{n+1}· (2)
2(n+2) ROW	O_{n+1} (1)	E_{n+2} (1)	O_{n+1} (2)	E_{n+2} (2)

FIG. 23

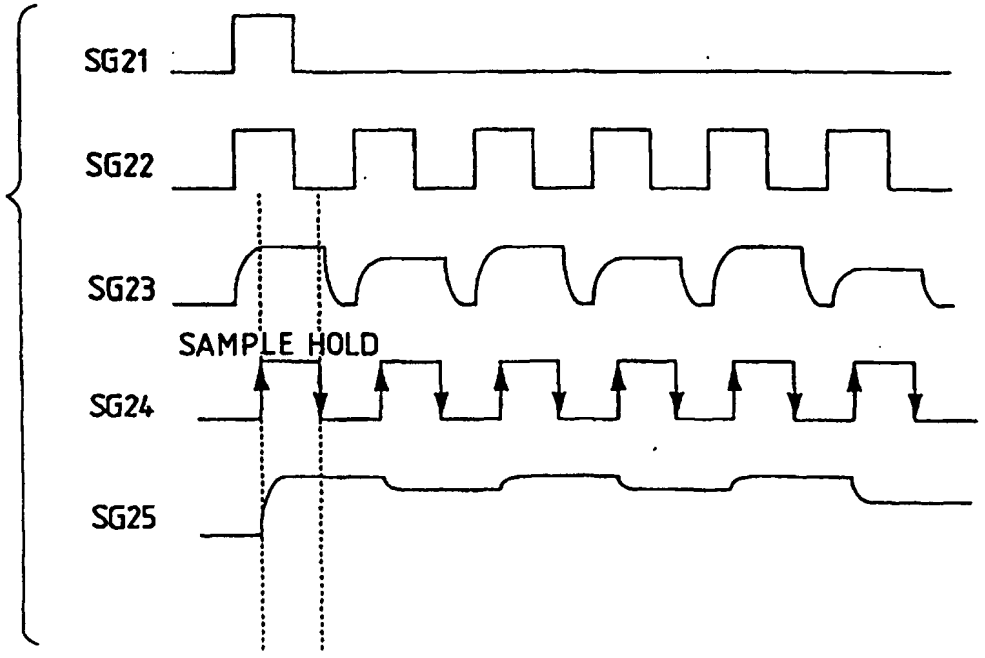


FIG. 24

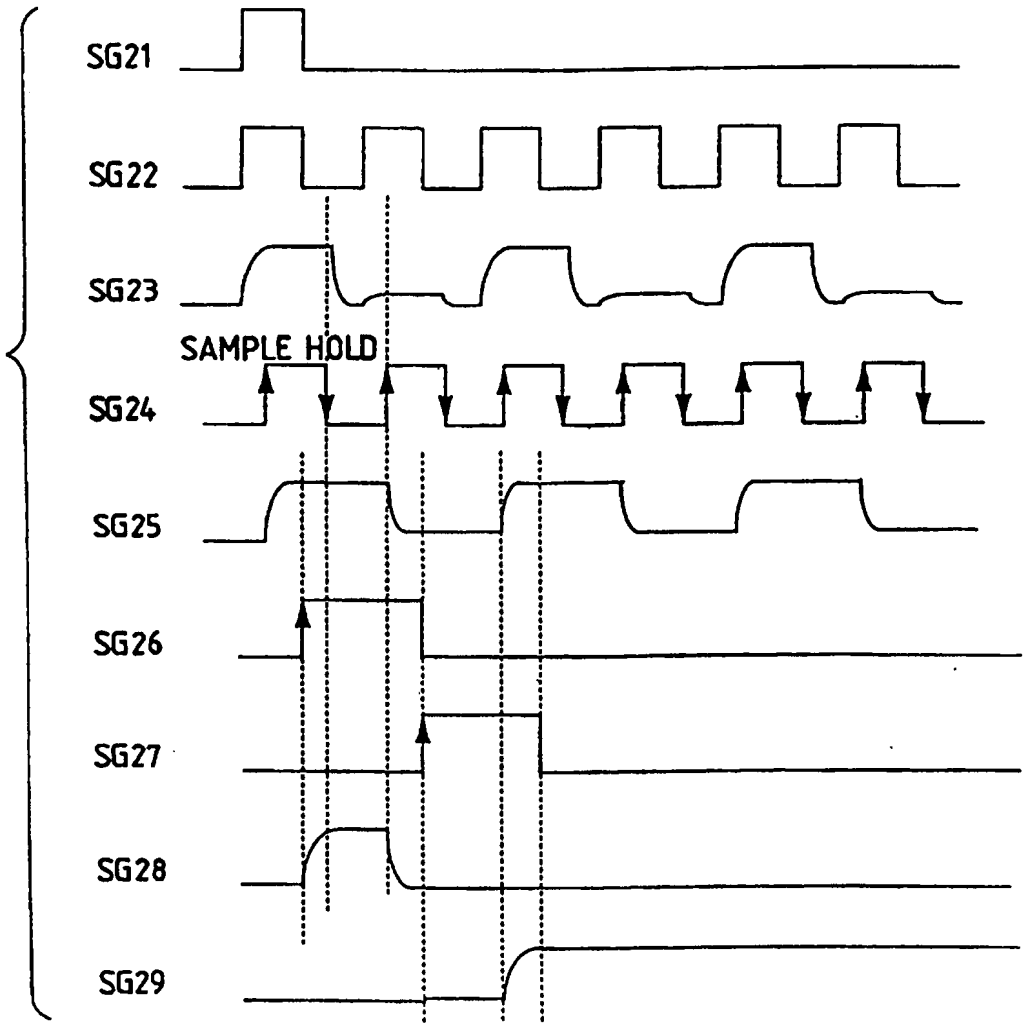
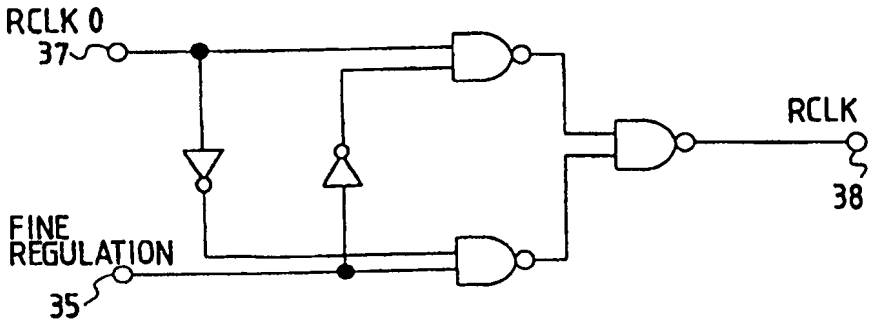

SG21
SG22
SG23
SAMPLE HOLD
SG24
SG25
SG26
SG27
SG28
SG29

FIG. 25


RCLK 0
37
RCLK
38
FINE
REGULATION
35

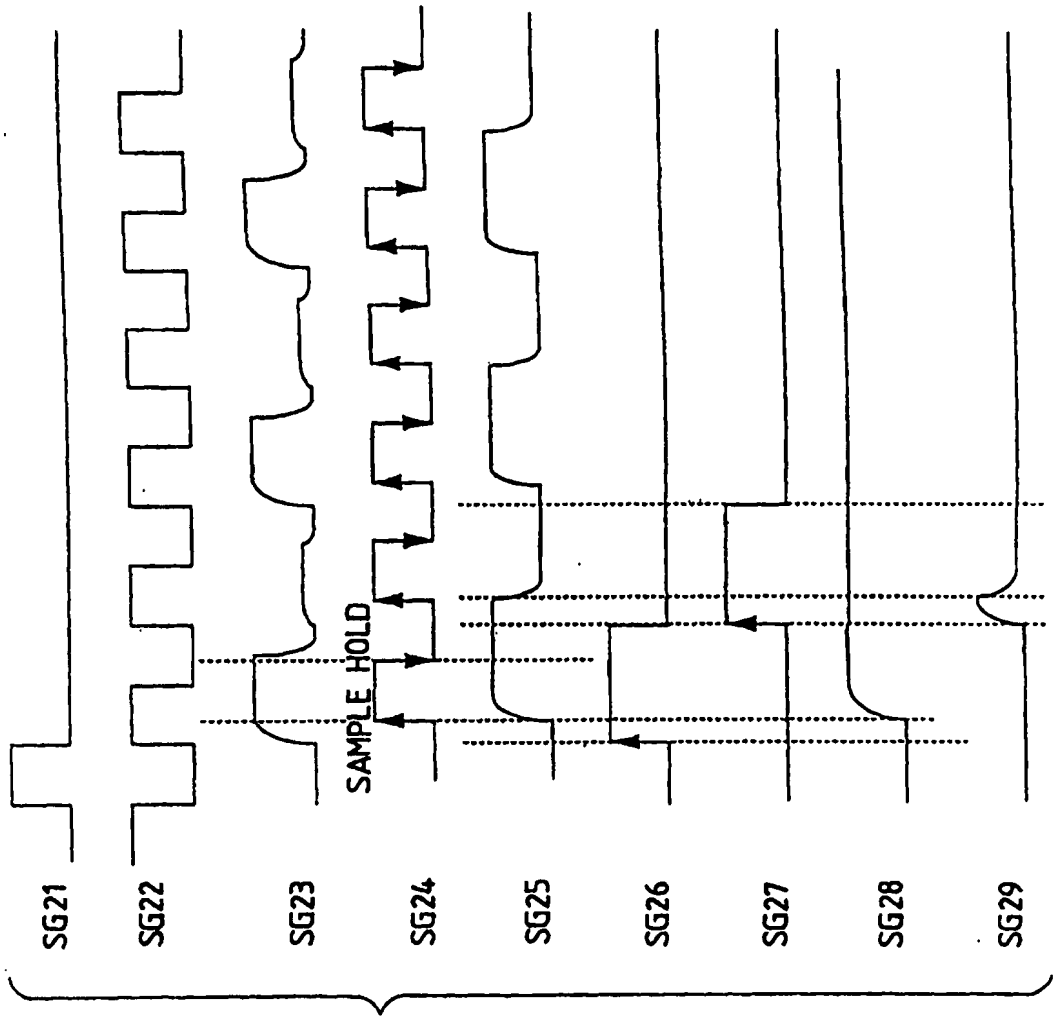


FIG. 26

FIG. 27

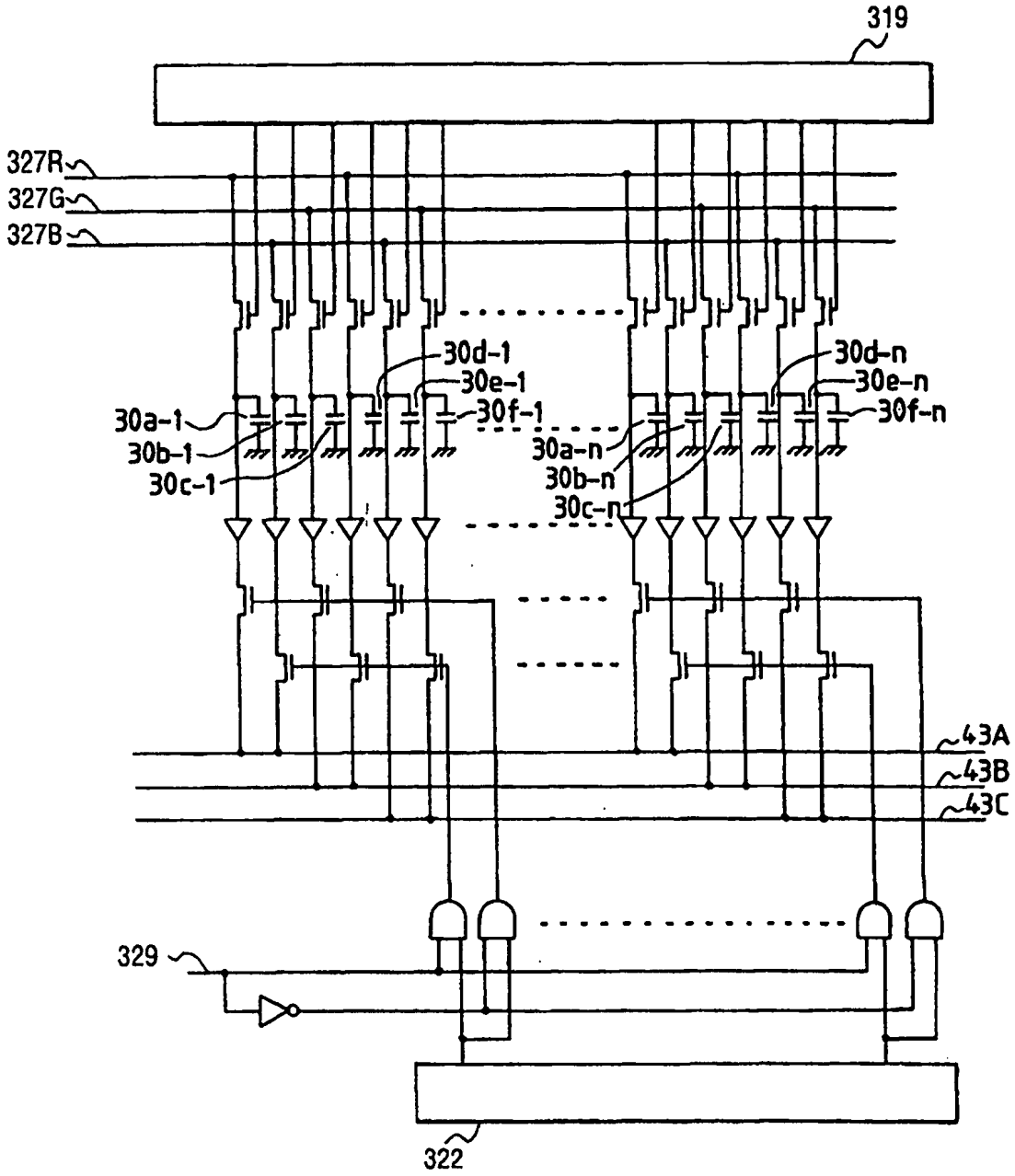
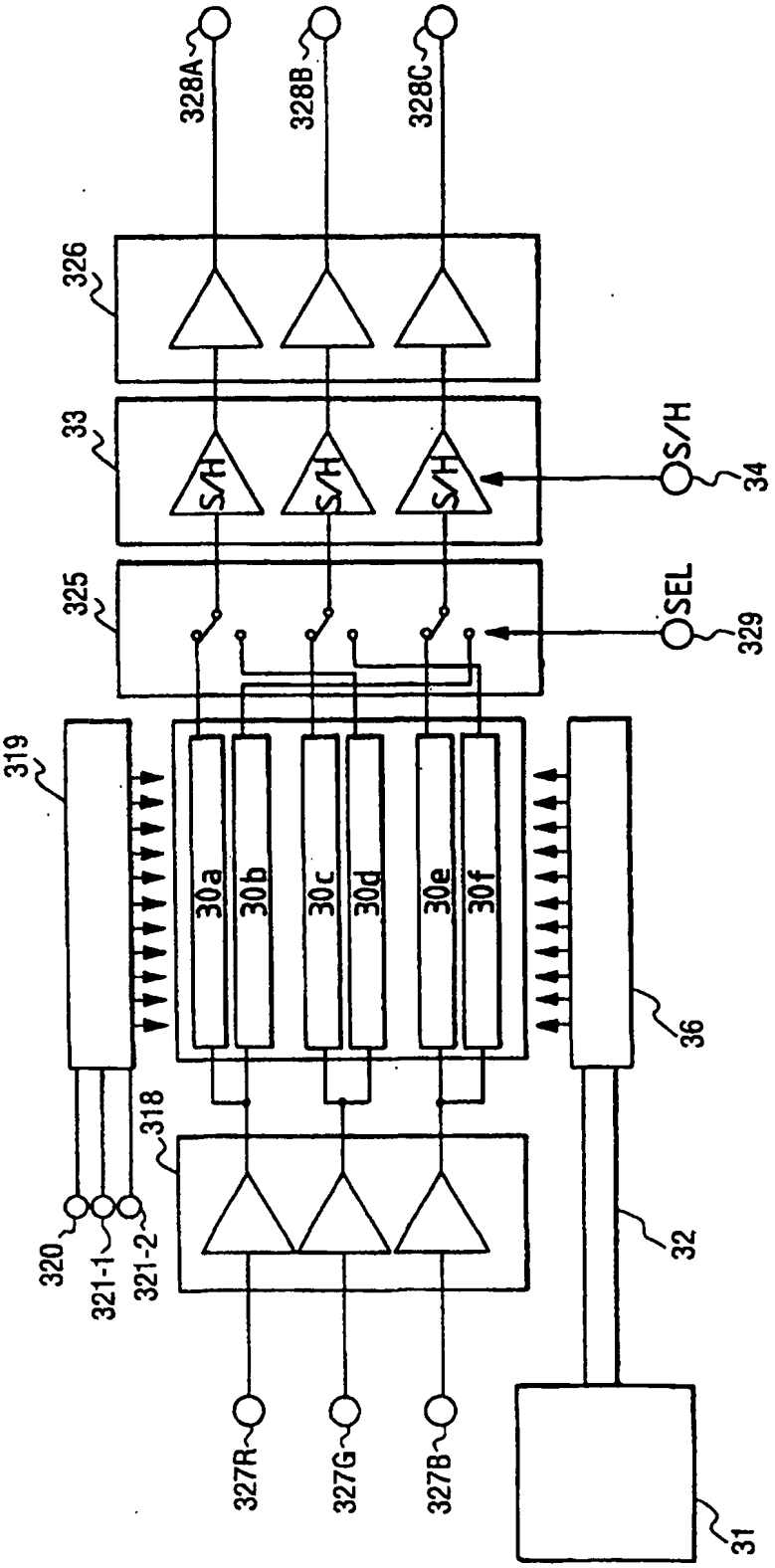

319
327R
327G
327B
30d-1
30e-1
30f-1
30a-1
30b-1
30c-1
30d-n
30e-n
30f-n
30a-n
30b-n
30c-n
43A
43B
43C
329
322

FIG. 28


328A
328B
328C
326
33
S/H
34
325
SEL
329
319
30a
30b
30c
30d
30e
30f
36
318
320
321-1
321-2
32
327R
327G
327B
31

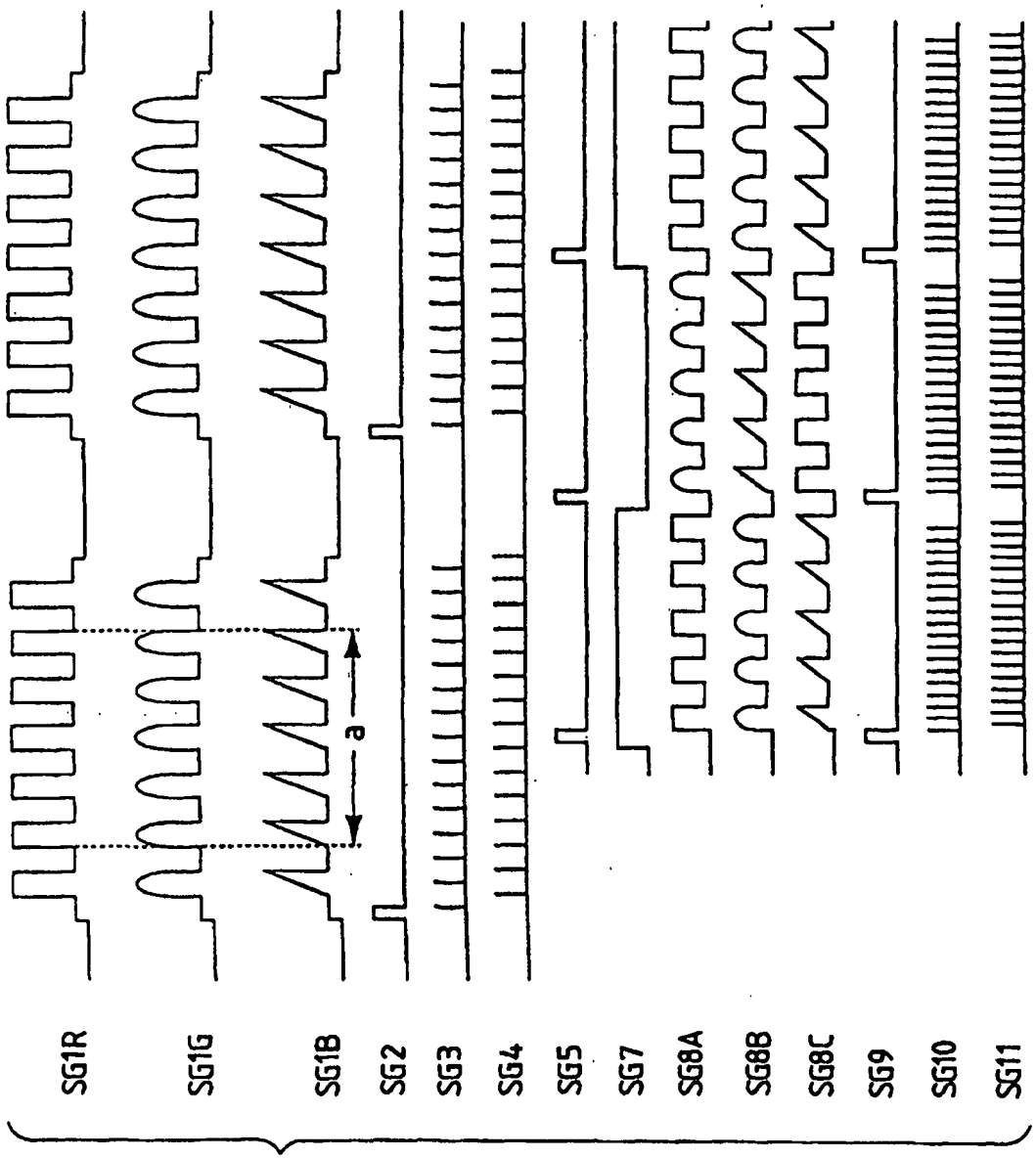

SG1R
SG1G
SG1B
SG2
SG3
SG4
SG5
SG7
SG8A
SG8B
SG8C
SG9
SG10
SG11
a

FIG. 29

FIG. 30A

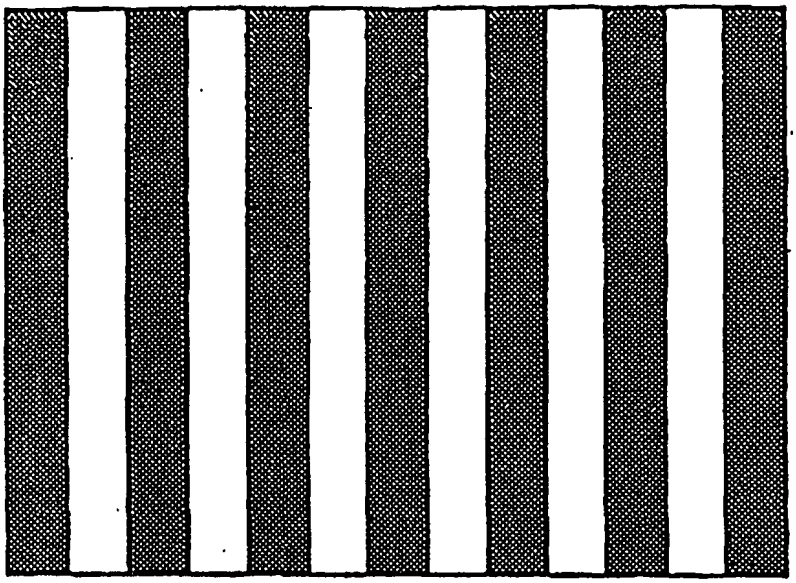


FIG. 30B

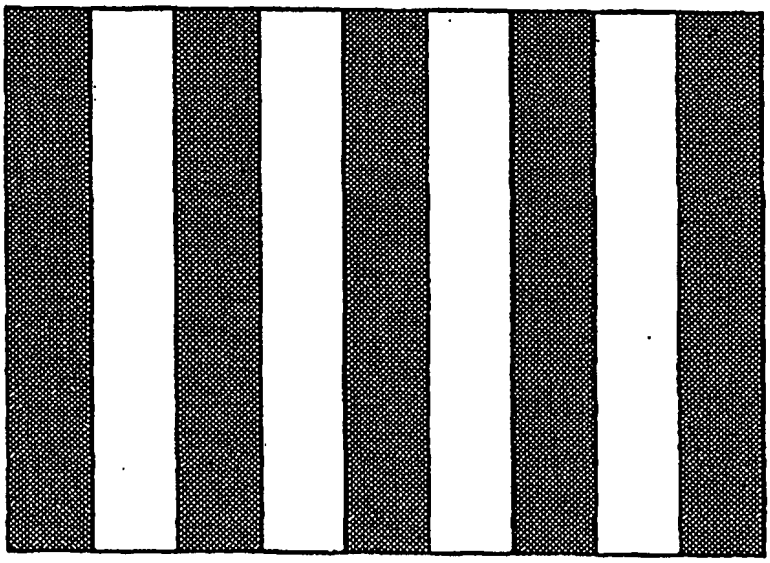


FIG. 31

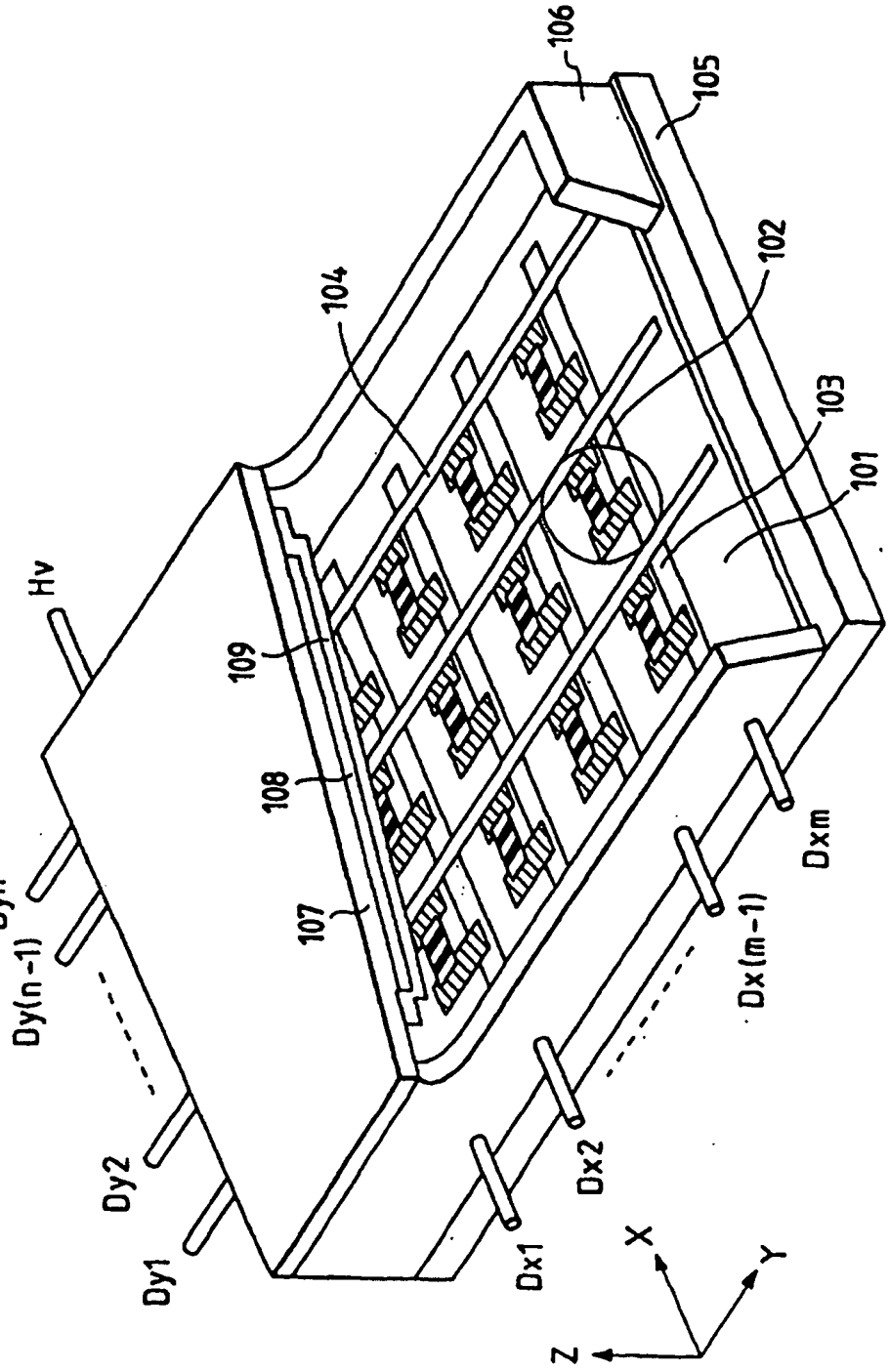

106
105
104
102
103
101
Hv
109
108
107
Dyn
Dy(n-1)
Dy2
Dy1
Dx1
Dx2
Dx(m-1)
Dxm
X
Y
Z

FIG. 32A

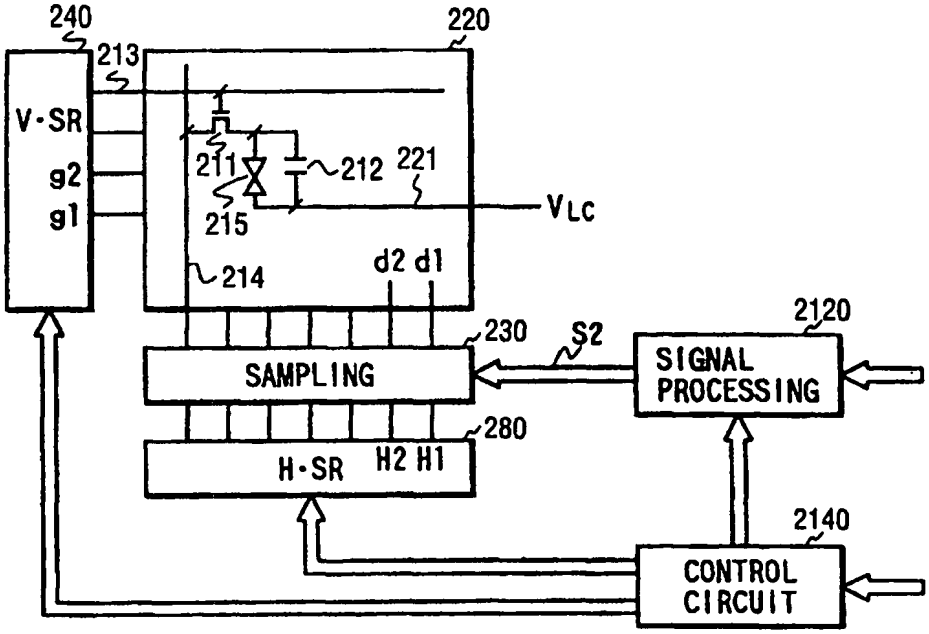


FIG. 32B

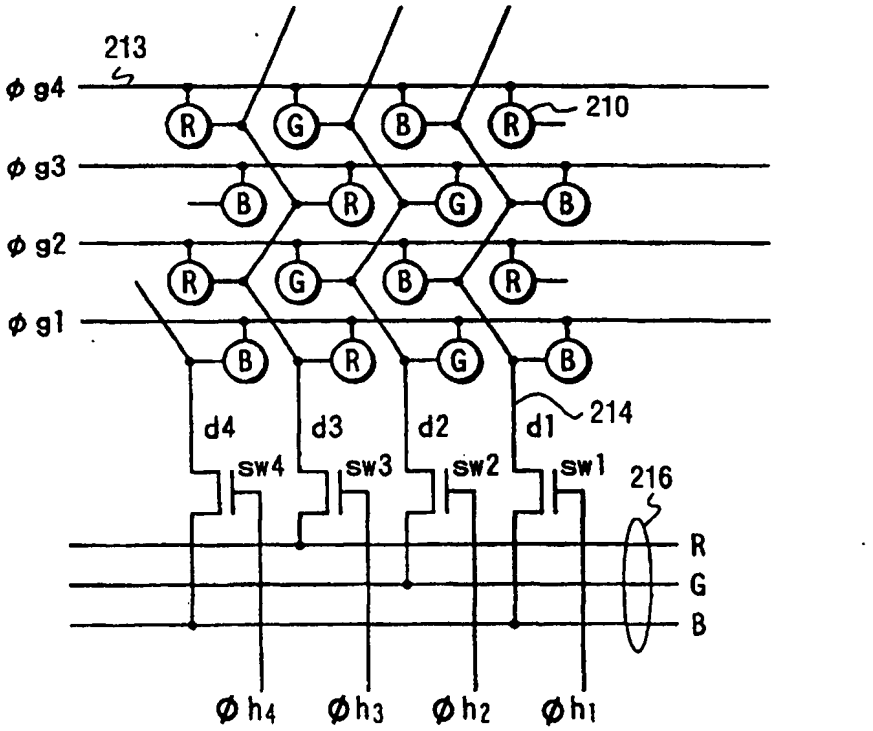


FIG. 33

ROW	IMAGE SIGNAL	
	ODD FIELD	EVEN FIELD
L1	o1 -	e1 +
L2	o2 +	e2 -
L3	o3 -	e3 +
L4	o4 +	e4 -
L5	o5 -	e5 +
L6	o6 +	e6 -
L7	o8 -	e7 +
L8	o9 +	e8 -
L9	o10 -	e10 +
⋮	⋮	⋮